National Library of Canada
Bibliothèque nationale du Canada

Canadian Theses Service
Service des thèses canadiennes

Ottawa, Canada
K1A 0N4

NOTICE

The quality of this microform is heavily dependent upon the quality of the original thesis submitted for microfilming. Every effort has been made to ensure the highest quality of reproduction possible.

If pages are missing, contact the university which granted the degree.

Some pages may have indistinct print especially if the original pages were typed with a poor typewriter ribbon or if the university sent us an inferior photocopy.

Reproduction in full or in part of this microform is governed by the Canadian Copyright Act, R.S.C. 1970, c. C-30, and subsequent amendments.

AVIS

La qualité de cette microforme dépend grandement de la qualité de la thèse soumise au microfilmage. Nous avons tout fait pour assurer une qualité supérieure de reproduction.

S'il manque des pages, veuillez communiquer avec l'université qui a conféré le grade.

La qualité d'impression de certaines pages peut laisser à désirer, surtout si les pages originales ont été dactylographiées à l'aide d'un ruban usé ou si l'université nous a fait parvenir une photocopie de qualité inférieure.

La reproduction, même partielle, de cette microforme est soumise à la Loi canadienne sur le droit d'auteur, SRC 1970, c. C-30, et ses amendements subséquents.

NL-339 (r. 88/04) c

Canada

University of Alberta

A WAFER FABRICATION ASSESSMENT MODEL BASED ON CLUSTERING OF IC FAILURE PATTERNS

by

MLADEN M. RAJHARD

A Thesis

Submitted to the Faculty of Graduate Studies and Research in Partial Fulfillment of the Requirements for the Degree of Master of Science

Department of Electrical Engineering

Edmonton, Alberta

Spring 1991

© Mladen M. Rajhard, 1991

National Library of Canada
Bibliothèque nationale du Canada

Canadian Theses Service
Service des thèses canadiennes

Ottawa, Canada
K1A 0N4

The author has granted an irrevocable non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of his/her thesis by any means and in any form or format, making this thesis available to interested persons.

The author retains ownership of the copyright in his/her thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without his/her permission.

L'auteur a accordé une licence irrévocable et non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de sa thèse de quelque manière et sous quelque forme que ce soit pour mettre des exemplaires de cette thèse à la disposition des personnes intéressées.

L'auteur conserve la propriété du droit d'auteur qui protège sa thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.

ISBN 0-315-66624-2

Canada

University of Alberta

Release Form

Name of Author: Mladen M. Rajhard

Title of Thesis: A Wafer Fabrication Assessment Model Based on Clustering of IC Failure Patterns

Degree: Master of Science

Year this Degree Granted: 1991

Permission is hereby granted to the University of Alberta to reproduce single copies of this thesis and to lend or sell such copies for private, scholarly or scientific research purposes only.

The author reserves other publication rights, and neither the thesis nor extensive extracts from it may be printed or otherwise reproduced without the author's written permission.

Mladen M. Rajhard
4207 117th Street
Edmonton, Alberta
T6J 1T5

Date: April 17, 1991

UNIVERSITY OF ALBERTA

Faculty of Graduate Studies and Research

The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled

A WAFER FABRICATION ASSESSMENT MODEL BASED ON CLUSTERING OF IC FAILURE PATTERNS

Submitted by: **Mladen M. Rajhard**

in partial Fulfillment of the Requirements for the Degree of **Master of Science**

Dr. Don Koval

Dr. Ljubisa Ristic

Dr. Jerry Leonard

Date: **December 13, 1990**

ABSTRACT

A WAFER FABRICATION ASSESSMENT MODEL BASED ON CLUSTERING OF IC FAILURE PATTERNS

This study presents a generalized model for the performance assessment of integrated circuit (IC) fabrication processes. The primary advantage of the proposed cluster model lies in its ability to provide quality confidence information about dies and wafers, while requiring only the standard die failure patterns as data. The relationship between the relative positions of dies and the pattern of die failure is explored. This relationship can be adequately represented by a Gaussian weighting function. The values from the model can be used to monitor the performance of a fabrication process over time.

This thesis discusses in some detail the current literature on the statistical assessment of the performance of wafers. The existing models include consideration of defects as randomly distributed points and the use of critical areas to determine yield. The thesis demonstrates the limitations of these concepts and how the proposed cluster model avoids many of these limitations.

A detailed example is presented in this thesis to demonstrate the cost reduction generated by the proposed model through early screening based on individual die cluster values.

Acknowledgments

This thesis was possible through the assistance and confidence of LSI Logic, Dr. Don Koval, and Dr. Ljubisa Ristic.

In the area of IC technology, very few companies are willing to place themselves at risk and provide information about their technology and processes. I was fortunate enough to have the assistance of LSI who provided information which greatly assisted the modelling aspects of this thesis.

Dr. Don Koval committed much time and energy into this project, both through the discussions of the concepts involved and in reviewing the many drafts. He provided many suggestions which greatly improved the flow of concepts within this thesis.

Dr. Ljubisa Ristic was instrumental in my developing interests in this area and assisted in the formulation of the concepts used. His suggestions provided for many improvements and the final form of the thesis stands more solid as a result.

Finally, I would like to thank my wife, Lorene, for her patience, encouragement, and good ear. I would like to thank her for the many times that she has been there to offer her support.

Table of Contents

Chapter 1

Introduction 1

Scope and Terms of the Thesis 4

Defining the Scope 4

Definition of Fabrication Terms 6

Definition of Performance Terms 8

Definition of Quality 8

Definition of Die Failure 9

Definition of Yield 9

Definition of Defect 10

The Die Testing Process 10

The Wafer Acceptance Stage 10

Chapter 2

Introduction 14

Quality Testing Results and their Interpretation 16

Die Independence 17

Sheet resistance 18

Chapter 3

Introduction 20

Demonstration of the Cluster Model using a 1-D Example 20

Overview of the Die Proximity Function for the 1-D Example 23

Overview of the Cluster Value for the 1-D Example 25

Overview of Analysis using Cluster Values for the 1-D Example 27

The Die Cluster Value and Infant Mortality 29

Development of the 1-D Wafer Cluster Value 31

The Cluster Model 32

Development of the 2-D Die Proximity Function 32

An Example of the 2-D Cluster Model 34

Overview of Analysis using Cluster Values for the 2-D Example 38
Development of the 2-D Wafer Cluster Value 39
Inside the Cluster Model 39
Objectives of the Proximity Factor Weighting Coefficients 39
Determining a Function for the Weighting Coefficients 40
The Inverse Distance Function 42
The Gaussian Function 44
Test Set for the Evaluation of the Functions 46
Comparison Method 49
Future Directions 54

Chapter 4
The Objectives of Existing Models 56
The Objectives of the Cluster Model 57
Models Based on Randomly Distributed Point Defects 57
Analysis of Poisson distribution for modeling point defects 58
Modifications to the Poisson distribution 63
Numeric Vertical Yield Mapping 68

Chapter 5
Introduction 71
Cost Saving Measures 71
Pre-encapsulation testing for marginal dies 72
Determining the Minimum Acceptance Level 73
Tracking of the Fabrication Progress 78

Chapter 6 80

References 82

Appendix
Tables used in the Development 84

Table of Contents for Figures and Tables

Figure 1. Progress of gate and device interconnect materials 2

Figure 2. The physical life cycle of a typical integrated circuit product 4

Figure 3. Failure distribution in IC products 5

Table 1. MIL-STD-883 screening process tests in sequence 6

Figure 4. A sample wafer after ATE testing 11

Figure 5. The flow of an on-wafer testing process 12

Figure 6. An example of the on-wafer testing process 13

Figure 7. Two wafers with identical yield and different die failure patterns 17

Figure 8. Wafer resistivity pattern with contours at 1% increments 18

Figure 9. Binary value assignment to wafer test data. 21

Figure 10. Development of the 1-D model from wafer data 22

Figure 11. Data for the 1-D example. 22

Figure 12. Equidistant sets for 1-D example 23

Figure 13. Tabulating the number of accepted dies in Set 1 24

Figure 14. Tabulating the number of accepted dies in Set 2 24

Table 2. Proximity factor results, F0, F1, F2, for die 1 (1-D) 24

Table 3. Proximity factor results for the first and second die (1-D) 25

Table 4. Proximity factor values for all the dies in the 1-D example 25

Table 5. Proximity factor and cluster values for the dies in the 1-D example 26

Figure 15. Cluster values for the 1-D data set in graphical form 27

Table 6. Ranking of the dies in the 1-D example based on the cluster values 28

Figure 16. Acceptance level for a particular application 29

Figure 17. Acceptance level for infant mortality reduction 30

Figure 18. Acceptance level for demanding applications 31

Figure 19. Equidistant sets for 2-D analysis 33

Figure 20. Calculation of proximity factors F0, F1 and F2 33

.c.Figure 21. An example wafer with nine dies 34

Figure 22. Determining proximity factors F0, F1, and F2 (2-D) 35
Table 7. Proximity factor values for all the dies in the 2-D example 36
Table 8. Proximity factor and cluster values for the dies in the 2-D example 37
Figure 23. Transition from binary data to cluster values..... 37
Figure 24. Example of a minimum acceptance plane..... 38
Figure 25. Examples of die failure clustering patterns. 40
Figure 26. Weighting coefficients φ produced from Sin(x)/x function..... 41
Figure 27. General form of the inverse distance function..... 42
Figure 28. Special form of the inverse distance function 43
Figure 29. General form of the Gaussian function..... 44
Figure 30. Control of the Gaussian function shape through modification of parameter σ 45
Figure 31. Gaussian function using σ = 1.40..... 46
Figure 32. The creation of a test set using the wafer number to generate a unique die layout 47
Figure 33. Analyzing of the first cell of wafer 98 to obtain the corresponding set of proximity factors..... 47
Figure 34. A sample of the set of die patterns used. 48
Table 9. A portion of the factor table for the 512 test wafers 48
Figure 35. Proximity factor and pattern equivalent wafers determined from pattern manipulations. 49
Table 10. A portion of the data for the 86 test wafers..... 50
Figure 36. Inverse Distance and Gaussian sort list in the order specified by the Inverse Distance function. 51
Figure 37. Enlarged view of the sort order based on Inverse Distance. 52
Figure 38. Test wafer patterns 106 and 45, and the corresponding proximity factors. 52
Figure 39. Relative contribution of each proximity factor 55
Table 11. Comparison of the Poisson model of yield to the binomial model..... 62
Figure 40. An example of partitioning two distinct theoretical zones of defect density on a wafer 63
Figure 41. Yield contour based on a sample wafer's die failure pattern 64

Figure 42. Particle maps obtained with an electronic particle detector 65
Figure 43. Particle counts from a grid analysis of patterns 1 and 8..... 65
Figure 44. The observed frequency of defects per cell superimposed upon the calculated expected values for pattern 1 66
Figure 45. The observed frequency of defects per cell and the calculated expected values for pattern 8..... 67
Figure 46. Vertical yield map..... 68
Figure 47. Numeric vertical yield map for 35 wafers 69
Figure 48. Surface rendering of the data..... 69
Figure 49. A set of 104 accepted dies from a wafer test ranked in descending order by cluster value..... 72
Figure 50. Final results recorded by orginal die position..... 74
Figure 51. The accepted dies are divided based on their cluster values 76
Figure 52. Financial return with increasing MAL..... 77
Figure 53. Using multiple MALs..... 78
Figure 54. A product hysteresis curve 79

CHAPTER 1

FACTORS IN THE PERFORMANCE ASSESSMENT OF IC FABRICATION

INTRODUCTION

To remain competitive in an aggressive semiconductor manufacturing market, integrated circuit (IC) facilities are continually striving to improve their fabrication processes. This is reflected by the current research into new methods and materials. Technological limits caused by the acceleration of failure mechanisms have only prompted the development of new techniques. This progress is illustrated in Figure 1, which also shows the submicron technology being investigated presently. The approximate minimum widths of each technology also are indicated.

The concerns over reliability have also prompted research in design (design for testability), and testing (detection, analysis, and elimination of failure mechanisms [1]). This thesis analyzes failure mechanisms at the earliest point in the integrated circuit life cycle, the circuit fabrication. The model proposed in this thesis assesses the performance of the circuit fabrication process by characterizing the clustering of failure patterns that occur on a finished wafer.

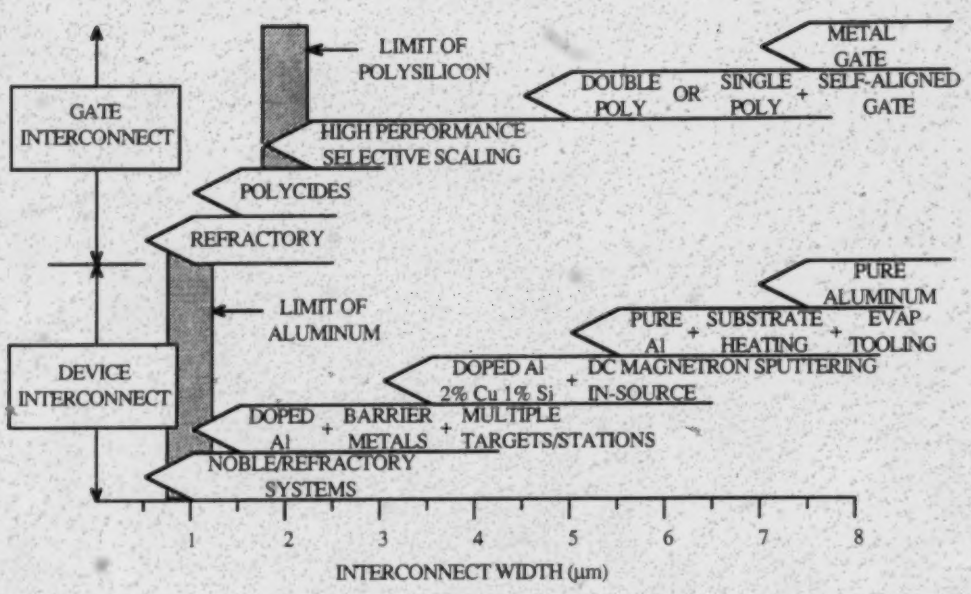


Figure 1. Progress of gate and device interconnect materials showing the minimum dimensions for each technology [2].

Using the proposed methodology, facilities could reduce costs on encapsulation and quality control testing, by rejecting potentially weak (but functional) circuits after the on-wafer circuit tests. The proposed methodology also could be used in the development of failure mode signature analysis such that manufacturers, could in the future, detect anomalies not normally uncovered by traditional testing methods. By correlating these anomalies with the various stages in the fabrication process, control could be improved.

The proposed model will augment current methods of assessing fabrication performance. In a later section, the means by which the model may be incorporated into a fabrication facility's testing structure will be shown.

To develop the model, various concepts were analyzed that pose problems to current methods of designing assessment models. These concepts, explained briefly here, will be examined and the specifications for the proposed cluster model will be developed from the analysis of these concepts.

First, binary values are used represent die yield. However, binary values cannot reveal the range of quality differences between dies. As a result, the separation of dies based on their quality is achieved through costly testing procedures.

Secondly, dies are considered independent from each other for the purposes of analysis and hence their arrangement on a wafer is not important. To most assessment methods, two wafers with the same yield will appear identical, even if the patterns of failure on the wafers are entirely different.

Lastly, many yield models and yield assessment tools are based on studies of defects rather than die yields. One defect process that is easily measured on wafer surfaces is particle contamination. As a result, many models are based on the patterns of distribution of particle defects. However, the transition from defect models to yield models is a difficult one since yield is affected by faults, a subset of defects that have an adverse effect on the structure of a circuit. The characteristics determined for defects do not necessarily hold for the characteristics of faults.

To overcome this transition, the concept of critical area was developed. Critical area is the subset of the die area that is used by signal lines and

operational devices. Thus, if a simulation study places a defect within a critical area, the defect would be considered a fault.

SCOPE AND TERMS OF THE THESIS

Defining the Scope

The diagram shown in Figure 2 shows the stages involved in the production and implementation of integrated circuit products. This thesis involves the areas indicated in bold with most of the emphasis on wafer processing, which involves fabrication of circuits on the wafer surface.

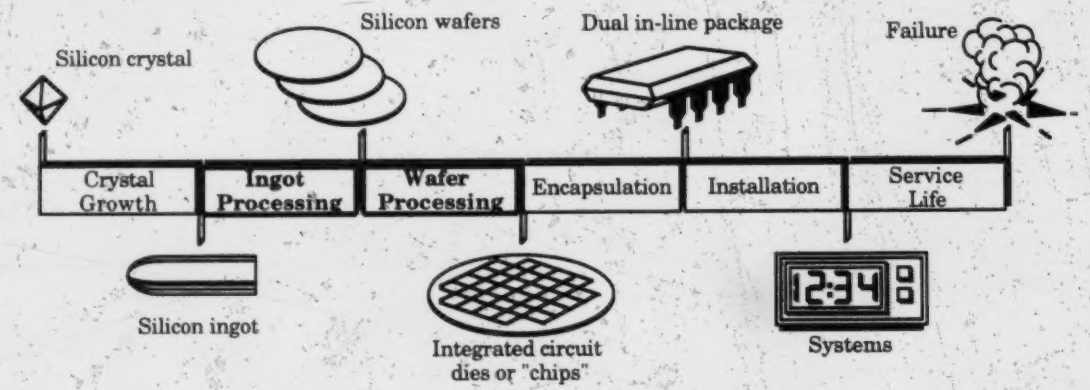


Figure 2. The physical life cycle of a typical integrated circuit product from the growth of the silicon ingot, and manufacturing to ultimate failure at some point in the future.

Further explanations of the fabrication process may be obtained from various texts [3, 4, 5].

A portion of integrated circuit products produced on every fabrication line have latent flaws that result in early failures under normal operating conditions. As a quality control measure, this portion of dies is induced to fail by using specially designed acceptance testing methods. The ICs that fail are part of the failure distribution known as "infant mortality". This is illustrated in Figure 3, with the two other stages of the failure distribution.

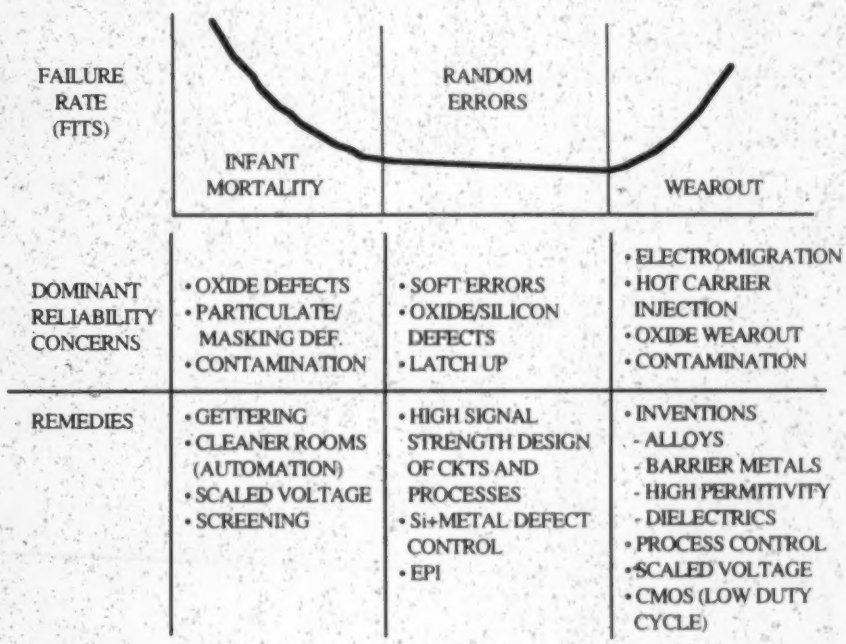


Figure 3. Failure distribution in IC products [6].

To control "infant mortality", and to ensure that a high quality product reaches the customer, the quality control for an integrated circuit involves a range of compliance tests. Table 1 outlines the tests, or screens listed in MIL-STD-883, Test Methods and Procedures for Microelectronics.

Table 1. MIL-STD-883 screening process tests in sequence [1].

(a) *AT THE MANUFACTURING SITE*
- (1) wafer lot acceptance
- (2) assembly die shear and bond-pull
- (3) precap visual and seal

(b) *AT THE MANUFACTURER, A TEST LABORATORY OR A QUALIFIED USER*
- (1) bake
- (2) temperature cycling
- (3) constant acceleration
- (4) fine leak
- (5) gross leak
- (6) PIND (particle impact noise detection)
- (7) serialization
- (8) electrical functional
- (9) burn-in
- (10) electrical functional (repeat)
- (11) parametric drift
- (12) fine leak (repeat test)
- (13) gross leak (repeat test)
- (14) final electrical functional
- (15) X-ray inspection
- (16) quality conformance
- (17) external visual inspection
- (18) QA preshipment, data review
- (19) package

While all facilities may not use the complete set of screens for their product line, every facility employs some form of quality assurance to prevent flawed components from reaching their customers.

The proposed methodology would be used following the step (a) (1) *wafer lot acceptance*, to eliminate as early as possible (and thus without further expense) integrated circuits that may not survive a facility's set of quality assurance tests.

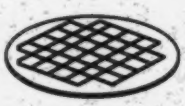
Definition of Fabrication Terms

The terms that will be most commonly used in this thesis are defined as follows.

Integrated Circuit: Commonly called a "chip" or IC, an integrated circuit is an electronic circuit whose components, such as resistors, capacitors, and transistors, are in the submicron to 10's of microns range. This allows the total chip area to be as small as several square millimeters while providing the functionality of discrete component circuits many orders larger in size.

Ingot: An ingot is a cylinder of electronic grade semiconductor crystal usually 10 to 15 cm in diameter, and up to 60 cm in length.

Wafer: A wafer is a circular slice cut from an ingot. One side is usually highly polished in preparation for processing integrated circuits. Wafers are usually processed in groups known as lots.



Dies: Upon completion of the circuit fabrication, the wafer carries a grid of integrated circuits. The circuits are referred to as dies while they are part of the wafer, and as chips when they are separated.

Dual in-line package: To provide physical protection from the environment, ICs are encapsulated in a plastic or ceramic enclosure. The most popular form of enclosure is the dual in-line package which has a row of electrical contacts on either side.

Definition of Performance Terms

To develop a method of assessing performance, it will be necessary to begin with the definition of various performance terms.

Definition of Quality

Quality will be defined as 'the totality of features and characteristics of a given product that bear upon its ability to satisfy a given need.' [1] The 'features and characteristics' will be the set of functional and parametric specifications (an agreed upon description of expected operation [7]) set by the facility and the customer. The 'given need' will be the definition of the use of an IC product in a particular function.

The definition of quality bears heavily upon the facility's criteria for defining die failure.

Definition of Die Failure

A die failure is the condition where the circuit operates outside a set of given specifications [7]. That is, the die functions either incorrectly or not at all, or some parameter varies outside a specified range.

Determining the exact specifications to dictate whether a die has failed and should be rejected, is still the subject of much debate and depends largely upon the operating specifications of the particular fabrication facility. In some instances, only degradation of the signals may occur although the chip continues to function correctly. Some manufacturers may consider this a failure, while others do not [1, 8].

Definition of Yield

Whether a tested die complies or fails to comply with the quality assurance specifications is referred to as the "die yield". This parameter is represented numerically by the binary values '1' or '0'. Dies that pass a set of compliance tests are called "accepted dies", while those which fail are called "rejected dies".

The total number of accepted dies on the surface of a wafer is defined as the "wafer yield". This yield value is either expressed as an integer or as a ratio of the number of accepted dies to the total number of dies on the wafer.

Definition of Defect

A defect in a die is the presence, absence, or modification of a physical form within the die. When a defect causes a failure in a die either by its nature or position, it also will be referred to as a fault. Thus, faults are a subset of all defects on a wafer. This definition will be important when discussing models and methods currently in existence since the characteristics determined for defects (which is often the case) may not necessarily hold for faults.

A defect, as defined here, will include common processing problems as small as dust particles and signal line breaks, or as large as improper ion implantation levels over an entire wafer. It will be understood that a defect may occur anywhere on the area of a die, on circuit patterns, on unused spaces, or on both if the defect is large enough. A defect also may be contained in the body of the wafer under the surface of the die. While many authors recognize that defects vary in size and form [9, 10], the most commonly used models to simulate yield use point defects that occur on the surface of the wafer [11, 12].

The Die Testing Process

The Wafer Acceptance Stage

After the circuit fabrication, the dies are tested according to MIL-STD-883 specification for wafer lot acceptance. The following is an overview of this test stage.

The uncut dies are evaluated with series of on-wafer tests using Automated Test Equipment (ATE) [13]. The ATE makes electronic contact with every die through fine probes, and applies a set of qualifying tests for the particular product. This includes testing the functions of the die, and measuring its electrical parameters. If a die fails any of the tests, it is marked with an ink dot. An example of a tested wafer with marked dies is shown in Figure 4.

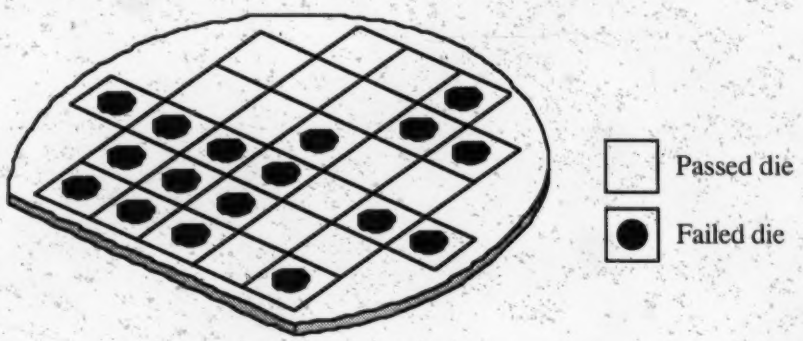


Figure 4. A sample wafer after ATE testing, showing failed dies marked with ink.

The process to arrive at the pattern shown in Figure 4 is demonstrated in Figure 5, which shows a possible sequence of three on-wafer tests; open and short circuit, general functionality, and output voltage level. To the right of the flowchart is the percentage of dies that could be encapsulated if the testing was concluded at that point. It follows then, that on-wafer testing could be extended, and this could reduce the final number of accepted dies.

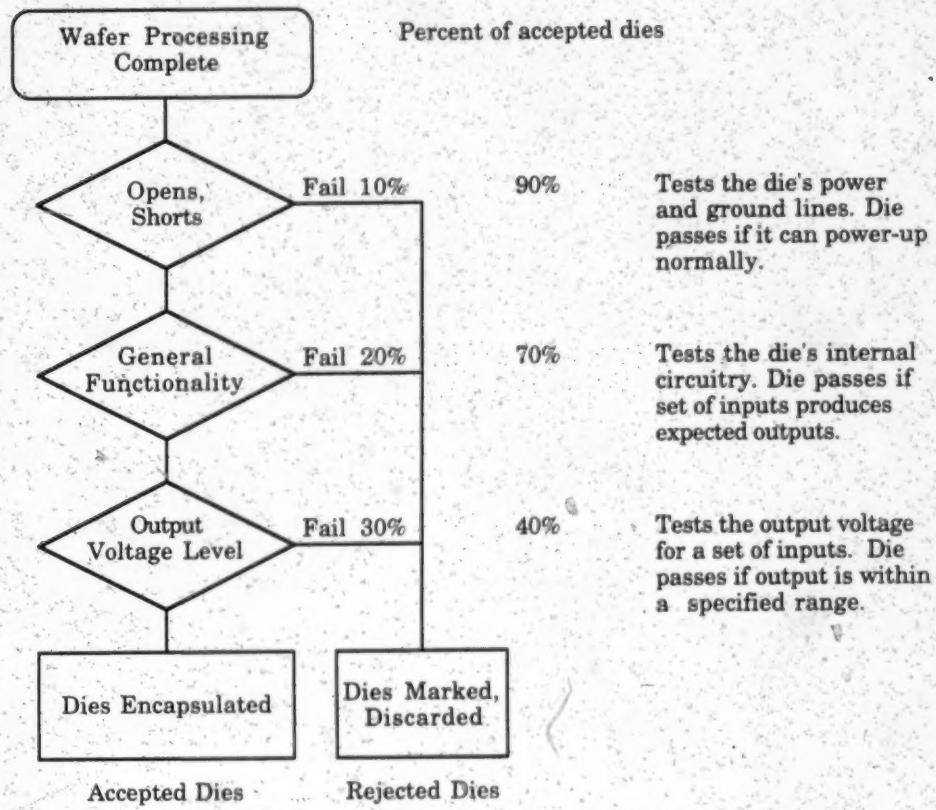

Wafer Processing Complete
Percent of accepted dies
Opens, Shorts
Fail 10%
90%
Tests the die's power and ground lines. Die passes if it can power-up normally.
General Functionality
Fail 20%
70%
Tests the die's internal circuitry. Die passes if set of inputs produces expected outputs.
Output Voltage Level
Fail 30%
40%
Tests the output voltage for a set of inputs. Die passes if output is within a specified range.
Dies Encapsulated
Dies Marked, Discarded
Accepted Dies
Rejected Dies

Figure 5. The flow of an on-wafer testing process consisting of three tests.

The wafer results at the end of each of the three tests are shown graphically in Figure 6. Dies that fail some prior test are not tested again.

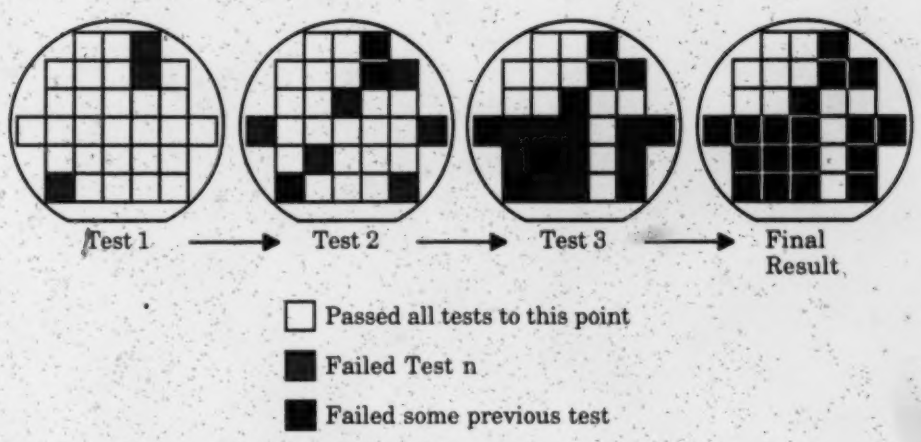


Figure 6. An example of the on-wafer testing process showing the progression of die rejection at each test stage.

The proposed methodology would accept the results of the wafer acceptance stage and analyze the patterns of die failure.

CHAPTER 2

RATIONALE FOR THE CLUSTER MODEL

INTRODUCTION

The models presented in much of the literature often originate from other fields of study. To adapt the models to the wafer fabrication field, the premises corresponding to the original model require transformation. Such transformations must always be done with extreme care, since the original and the present fields of study may contain an inherent set of principles that are considerably different. In the original context, a model may have accounted for the necessary factors to produce accurate results. However, a second field may contain factors that may not be accounted for in the original model and thus inaccurate results are produced.

The theory of quality and reliability in the wafer fabrication field is an extension of traditional manufacturing concepts. While much of the theory applies, the original manufacturing context involves the production of finished pieces that are produced independently. As a result, the theory was designed to analyze populations of independent items or events. Relationships exist in the wafer fabrication field that should be accounted for in models and assessment tools in order to produce accurate results.

The two types of relationships within the scope defined for this thesis are i) the relationship between the wafers that are produced from the same ingot, and ii) the relationship between integrated circuits produced from the same wafer. These are briefly explained below.

Wafers are sliced from an ingot and therefore inherit the crystal structure (including any crystal defects), and any imbedded impurities. By the very nature that wafers are cut from one ingot, an association is established between consecutive wafers.

Similarly, integrated circuits inherit the crystal structure and impurity level that exists in the area that they occupy on the wafer. Since crystal structures and impurity levels may vary across the wafer [14], circuits from localized areas of the wafer should exhibit similar electrical parameters such as threshold voltage, while circuits from separate areas could have large differences in these parameters. Thus, an association is established between circuits in neighbouring grid locations. As well, environment conditions may affect only localized areas. A section of the wafer may be exposed to contaminants or be subject to stresses that affect a localized group of circuits, but not those in a remote area of the wafer.

These relationships are not considered in typical manufacturing models and typical wafer fabrication models do not account for them. The proposed cluster model will incorporate the relationships between circuits to provide a method of assessment of the fabrication quality. The sections that follow analyze these relationships and establishes the criteria for the structure of the proposed model.

QUALITY TESTING RESULTS AND THEIR INTERPRETATION

The result of present die tests is either an acceptance or a rejection of a particular die based on whether the die can perform a set of functionality tests properly and whether the various electrical parameters are within the tolerable limits. This amounts to comparing the die's quality to the facility's standard or ideal. The binary values '1' and '0' represent quality levels above the minimum standard and below the minimum standard respectively. However, such a result cannot reflect the range of variation between the dies that pass the set of compliance tests. That is, an assignment of '1' implies that a die meets or exceeds the quality level required by the facility, but provides no indication of how much the die quality is above the minimum acceptable quality level.

To be accepted, a die may have any value for a tested parameter, so long as that parameter is within the stated bounds. Under present testing methods, the levels of these variations are usually ignored and all accepted dies appear to have identical test results. Thus all accepted dies would appear to be of equal quality.

As a result, a method is required to produce real-valued numbers to allow for improved fabrication assessment. Since the data from each test is not kept, the proposed cluster model will assign a value based on the yield results of the dies in the local area.

DIE INDEPENDENCE

Similar to the traditional manufacturing concept, the test result for a die is considered to represent the quality of only the tested die, and the quality of the tested die is assumed to be independent of all the other dies on the wafer. This precludes the possibility of the test results for one die being associated with those of nearby dies, even though the tests were not necessarily designed in that manner. If dies are considered independent of each other, this implies that their arrangement on a wafer is not important. Hence, two wafers with the same yield would be considered identical even if the patterns of failure on the wafers is different.

Figure 7, is an example of two wafers, with the same yield of 50%.

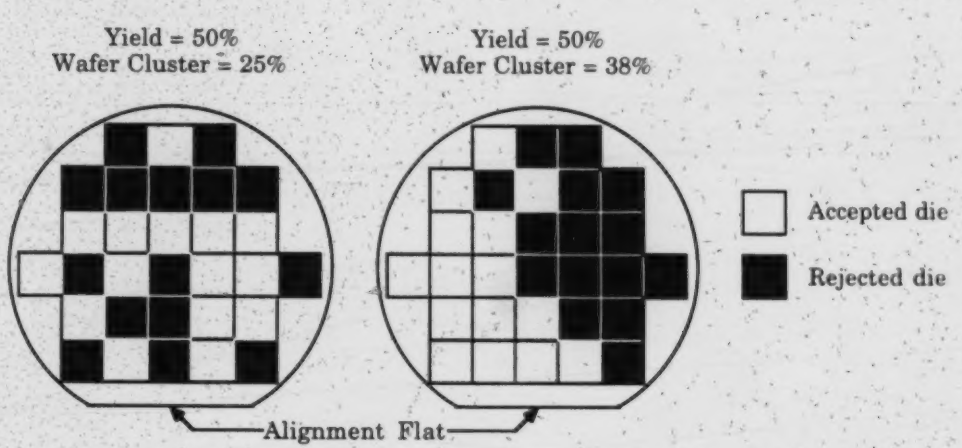


Figure 7. Two wafers with identical yield and different die failure patterns. Shown as well are the results of the cluster model analysis for each wafer.

For the dies from both wafers to be of equal quality requires that the faults that caused the die failures are smaller than the size of a die (to ensure independence between dies), and that the distribution of failures is

uniformly random (to ensure all wafer regions are identical). However, dies may be affected by influences that are neither smaller than a die nor distributed randomly over the wafer. Consider the example of wafer sheet resistance.

Sheet resistance

Wafers tend to exhibit sheet resistance variations across their surface as a result of the ingot growth process. The variations in sheet resistance affect the dielectric breakdown [15], current, voltage, and other parameters essential for normal operation of integrated circuits.

Ingots grown by the Czochralksi technique, exhibit impurity variations in both axial and radial resistance. When the ingot is sliced straight across its diameter into wafers, the variations, form a resistivity pattern unique to every wafer.

An example of one pattern is shown in Figure 8.

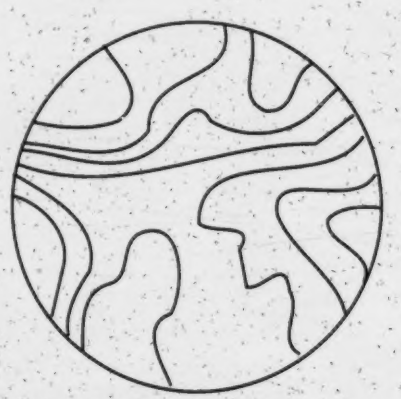


Figure 8. Wafer resistivity pattern with contours at 1% increments [16]

The proposition is made that dies should not be considered independent since factors that affect die yield are not necessarily randomly distributed or physically smaller than a die. Thus, the concept of analyzing the arrangement of accepted dies is proposed to be an important part of assessing the fabrication process that produced the wafer.

CHAPTER 3

THE CLUSTER MODEL

INTRODUCTION

The purpose of the proposed model is to assess the performance of the fabrication process by characterizing the die failure patterns that occur on a finished wafer. By revising the understanding of the die testing process and the produced results, it is possible to develop a procedure to analyze a wafer's failure patterns, and provide a guide to improving fabrication performance.

The proposed procedure produces a value that represents the failure pattern on the wafer. This value may be used to clarify the binary (accepted/rejected) information provided by the die testing process. This measure will be referred to as the cluster value, and it is one that could become an important tool in developing quality confidence intervals for individual dies as well as forming a numerical basis for comparing wafers.

Demonstration of the Cluster Model using a 1-D Example

To introduce the concepts used in the cluster model, a one-dimensional example will first be presented. This example will start at the end of the wafer acceptance stage. The areas covered will be the development of the

die proximity function, the assignment of the cluster value for a die and a wafer, and finally examples of the use of the model.

The one-dimensional data will be obtained from a single row of dies from a hypothetical wafer. After a wafer has passed through the wafer acceptance stage, the accepted dies will be assigned the value of '1' and the rejected dies will be assigned '0'. This is illustrated in Figure 9.

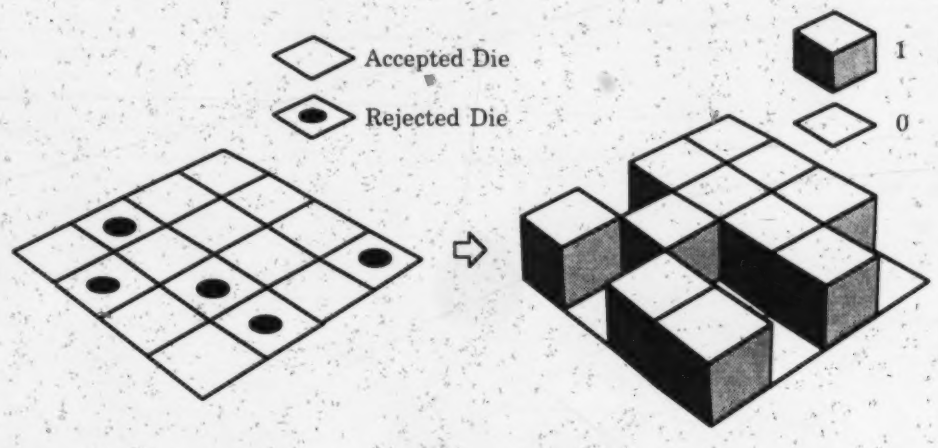


Figure 9. Binary value assignment to wafer test data.

To show yield data from a wafer in a simpler form, a bar chart will be used to reflect the yield of each die (1 or 0) in a row.

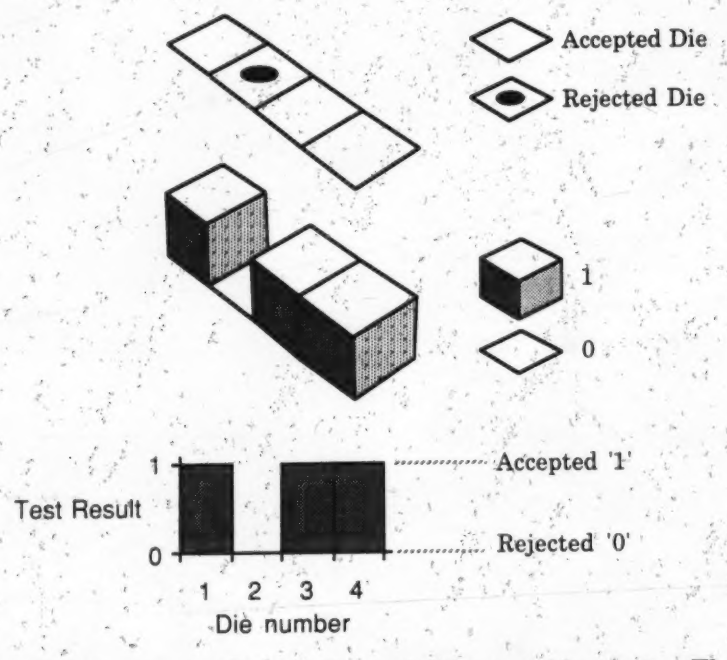


Figure 10. Development of the 1-D model from wafer data. The bar chart represents the yield of each die in a row as determined by the ATE.

The specific data that will be used to develop the model is shown in Figure 11. A row of 10 dies will be used, of which 6 have passed the compliance tests and 4 have failed.

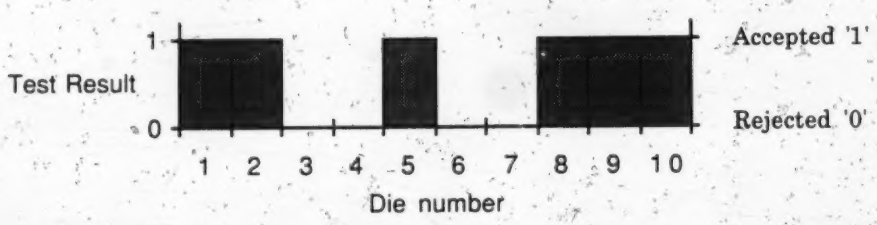


Figure 11. Data for the 1-D example.

Overview of the Die Proximity Function for the 1-D Example

The analysis begins by tabulating the proximity of the dies surrounding die 1. The tabulation is used to produce proximity factors (F_0, F_1, F_2, ...) which will be used in subsequent calculations. Each die is analyzed in turn, and the currently analyzed die will be referred to as the reference die.

The proximity factor F_0 is equal to the binary value of the reference die, and for die 1, F_0 is 1. Subsequent proximity factors, F_1, F_2, ..., are the total number of accepted dies contained in equidistant sets from the reference die. Set 1 is defined as those dies that are immediately adjacent to the reference die. Set 2 is defined as the set of dies that are two dies away from the reference die. Three sets are illustrated in Figure 12.

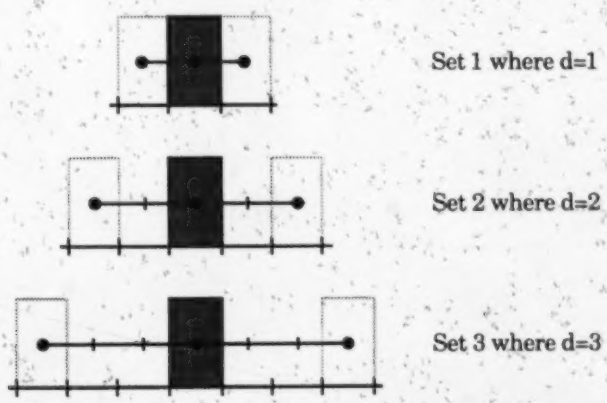


Figure 12. Equidistant sets for 1-D example. Each set consists of 2 dies an equal distance from a reference die. The value for the corresponding proximity factor is equal to the number of accepted dies in the set.

The number of sets may be made arbitrarily large. In this example, only Set 1 for proximity factor F_1, and Set 2 for proximity factor F_2 will be used.

Proximity factor F_1 for the first die is 1 since there is only one accepted die immediately adjacent to it.

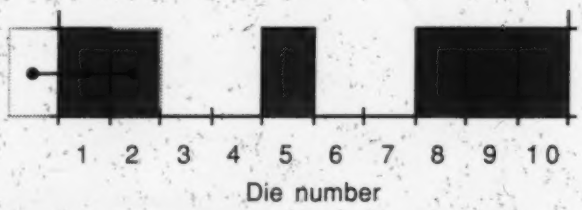


Figure 13. Tabulating the number of accepted dies in Set 1 with die 1 as the reference die (1-D).

Proximity factor F_2 is 0 since there are no accepted dies two dies away from the first die.

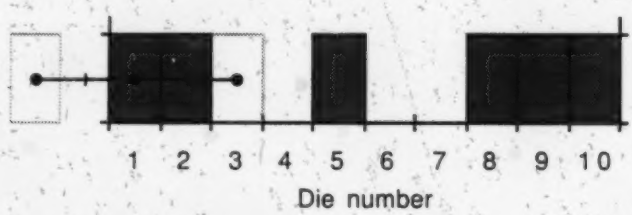


Figure 14. Tabulating the number of accepted dies in Set 2 with die 1 as the reference die (1-D).

When dies are on or near the edge of a wafer, as for die 1, the equidistant sets may extend past the edge, and hence past the point where data is available. In that case, the 'dies' past the edge are assigned a value of '0' representing 'rejected dies'.

The results for the first die are shown in Table 2.

Table 2. Proximity factor results, F_0, F_1, F_2, for die 1 (1-D).

Die	F_0	F_1	F_2
1	1	1	0

The next die, die 2 is designated the reference die and the tabulation process is repeated. Proximity factor F_0 is 1, since die 2 is an accepted die. Proximity factor F_1 is 1, since there is only one accepted die immediately adjacent to die 2, i.e., die 1. Proximity factor F_2 is 0 since there are no accepted dies two dies away.

Table 3. Proximity factor results for the first and second die (1-D).

Die	F_0	F_1	F_2
1	1	1	0
2	1	1	0

The tabulation process continues through to the last die, here die 10. The die proximity factors for this row of dies are shown in Table 4.

Table 4. Proximity factor values for all the dies in the 1-D example.

Die	F_0	F_1	F_2
1	1	1	0
2	1	1	0
3	0	1	2
4	0	1	1
5	1	0	0
6	0	1	1
7	0	1	2
8	1	1	1
9	1	2	0
10	1	1	1

Overview of the Cluster Value for the 1-D Example

In order to assign a cluster value to each die, the proximity factors determined for each die are weighted with a set of coefficients. The cluster value for the i^{th} die will be evaluated by Equation 1 where the

number of terms in the cluster function is equal to the number of proximity factors determined for each die.

$$c_i = \varphi_0 F_0 + \varphi_1 F_1 + \varphi_2 F_2 + \varphi_3 F_3 + \ldots = \sum_{j=0}^{n} \varphi_j F_j \qquad (1)$$

For now, the weighting coefficients φ_0, φ_1, φ_2 will be arbitrarily assigned the values 1, 0.75, and 0.25 respectively for illustration purposes only. Table 5 contains the proximity factors for each die and the cluster value based on the given weighting coefficients.

Table 5. Proximity factor and cluster values for the dies in the 1-D example.

Die	F_0	F_1	F_2	c_i
1	1	1	0	1.75
2	1	1	0	1.75
3	0	1	2	1.25
4	0	1	1	1.00
5	1	0	0	1.00
6	0	1	1	1.00
7	0	1	2	1.25
8	1	1	1	2.00
9	1	2	0	2.50
10	1	1	1	2.00

Graphing the individual cluster values above the individual yield values for the ten dies produces the graph in Figure 15.

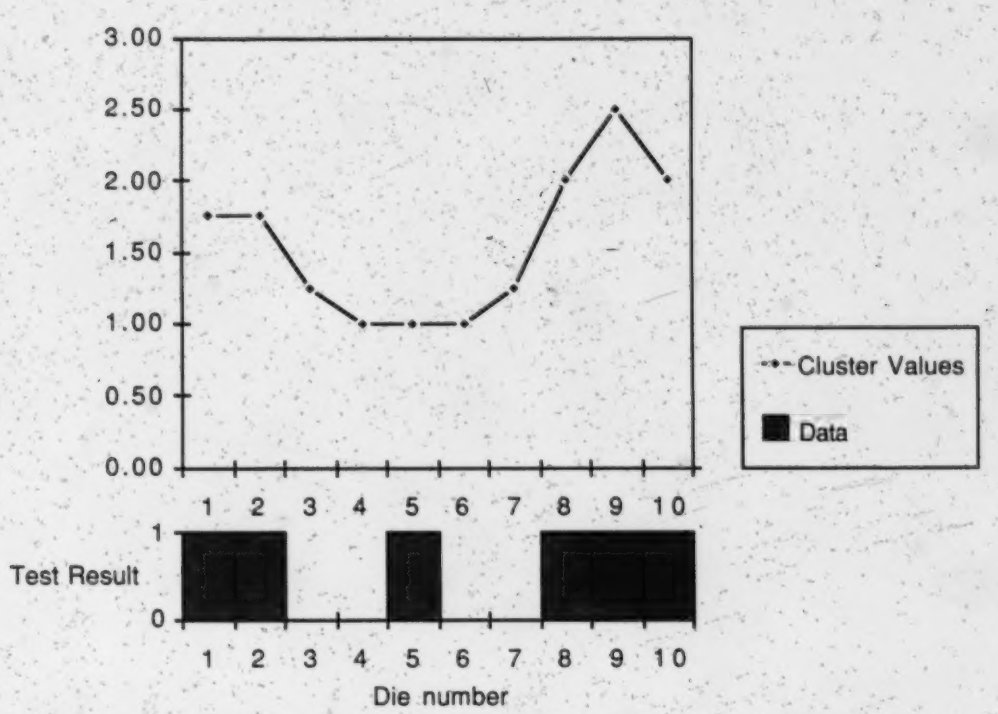


Figure 15. Cluster values for the 1-D data set in graphical form. The cluster value graph is aligned with the yield values for the data set.

Visually, the curve reflects the clustering of the die failure patterns. The cluster value for a die is high when positioned in close proximity to accepted dies. Conversely, the cluster value will be low when a die is in a region of rejected dies. The exact level of the cluster value for each die depends upon the values chosen for the weighting coefficients φ_0, φ_1, φ_2.

Overview of Analysis using Cluster Values for the 1-D Example

It is possible to analyze dies that were previously described only in terms of an accepted/rejected label with respect to their cluster values. If the dies in this example are ranked according to their cluster value, as shown

in Table 6, a facility can determine which dies to encapsulate and which to reject.

Table 6. Ranking of the dies in the 1-D example based on the cluster values.

Rank	Die	c_i
1	9	2.50
2	8	2.00
3	10	2.00
4	1	1.75
5	2	1.75
6	3	1.25
7	7	1.25
8	4	1.00
9	5	1.00
10	6	1.00

For instance, a facility may determine a cutoff point in the form of a minimum acceptable cluster level for accepting dies for a particular application. Figure 16 shows an example with the minimum acceptance level (MAL) set to 1.50. Dies with cluster values above 1.50 (dies 1, 2, 8, 9, and 10) would continue through the rest of the fabrication process while the rest would be rejected or packaged for less demanding applications.

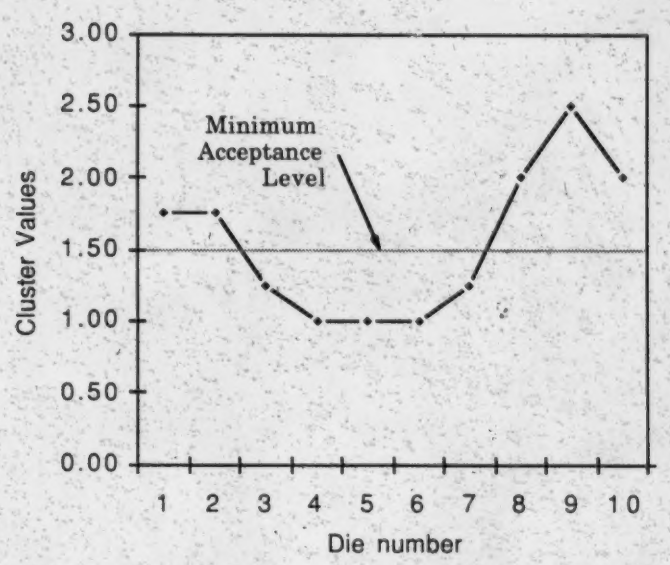


Figure 16. Acceptance level for a particular application.

The Die Cluster Value and Infant Mortality

The cluster value for each die indicates its proximity to other accepted and rejected dies. The lower the cluster value for an accepted die, the closer is its position to an area of rejected dies. If any of the die failure mechanisms extend past the edges of the rejected dies, the accepted dies close by could be affected. It follows that accepted dies with low cluster values may be correlated to dies contributing to infant mortality rates in finished products. Setting the MAL to a low value could result in cost savings of further processing by rejecting these dies at the wafer test stage. Figure 17, shows an example of the minimum acceptance level set to 1.25 to stem infant mortality. For this data set, all but three of the dies would be accepted and processed further.

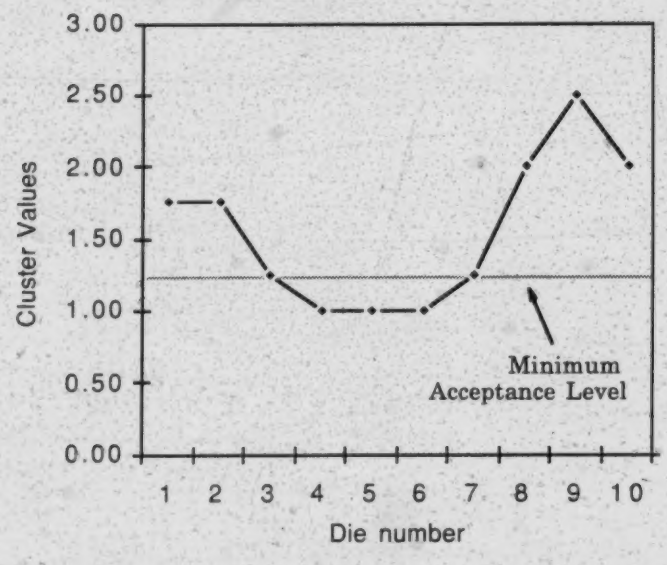


Figure 17. Acceptance level for infant mortality reduction.

For demanding environments such as military applications, facilities could set the acceptance level to an extremely high value, 2.75 for instance. Only dies with cluster values higher than this level would be considered for these applications. All other dies could be packaged for less demanding environments. Figure 18 shows that the entire example data set would be rejected for such an application.

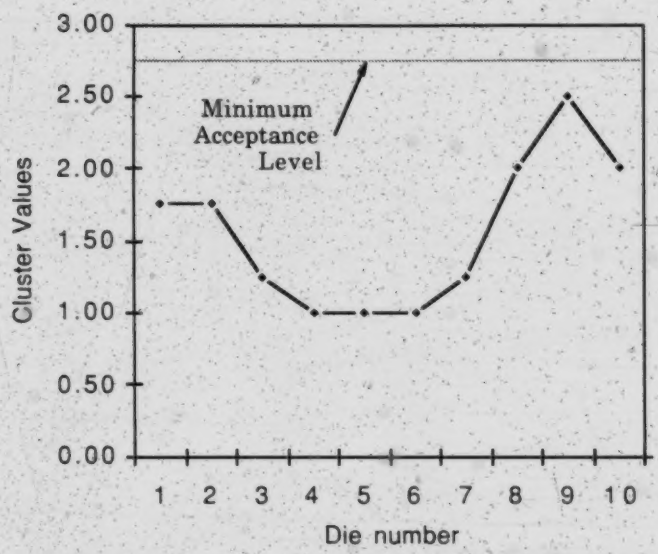


Figure 18. Acceptance level for demanding applications.

This type of evaluation may result in significant cost reductions for highly demanding applications that normally test large volumes of ICs in order to accept just a few. The cost reduction also could be supplemented by the sales of dies that would normally be destroyed in the intense testing process for less demanding applications.

The cluster method not only facilitates the analysis of dies but also has the capability of analyzing wafers and the progress of the fabrication process over time.

Development of the 1-D Wafer Cluster Value

The wafer cluster value is produced by the addition of the cluster value of each die multiplied by the die's F_0 term. This is equivalent to the summation of the cluster values for only the accepted dies (whose F_0

values are 1). The wafer cluster function for the k^{th} wafer will take the form of Equation 2 where N is the number of dies on the wafer.

$$wc_k = \sum_{i=1}^{N} F_{0_i} \times c_i \qquad (2)$$

The objective of the wafer cluster value is to reflect the level of grouping of the accepted dies for a particular wafer. This enables wafers to be compared and ranked thus enabling the fabrication process to be evaluated over time.

THE CLUSTER MODEL

Development of the 2-D Die Proximity Function

The 2-D die proximity function performs the same operation for a matrix of dies as the 1-D die proximity function does for a row of dies. The equidistant sets for calculating the proximity factors are now two-dimensional. Set 1 is defined as those dies that are immediately adjacent (one die unit measured centre to centre) to the reference die. Set 2 is defined as the set of dies whose centres are a distance $\sqrt{2}$ from the reference die centre. The first five sets are shown in Figure 19.

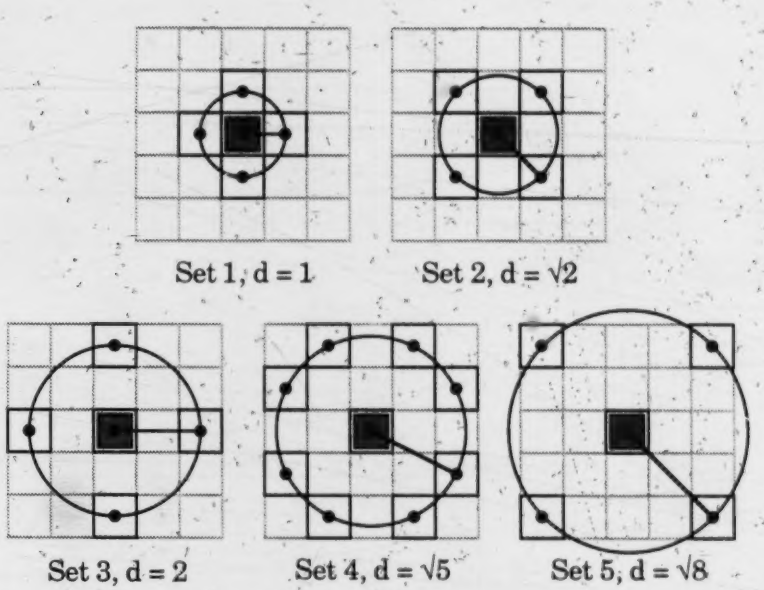


Figure 19. Equidistant sets for 2-D analysis.

The proximity factors are determined in the same manner as they were for the 1-D case. The proximity factor F_0 is equal to the binary value of the reference die. The number of accepted dies in each equidistant set is totalled to produce the proximity factors F_1, F_2, and so on. In Figure 20, a die pattern is shown where the centre die is designated as the reference die. The die proximity function would produce 1 for F_0 since the reference die is an accepted die. The number of accepted dies in Set 1 is 3. Thus, F_1 is 3. The number of accepted dies in Set 2 is only 1. Hence, F_2 is equal to 1.

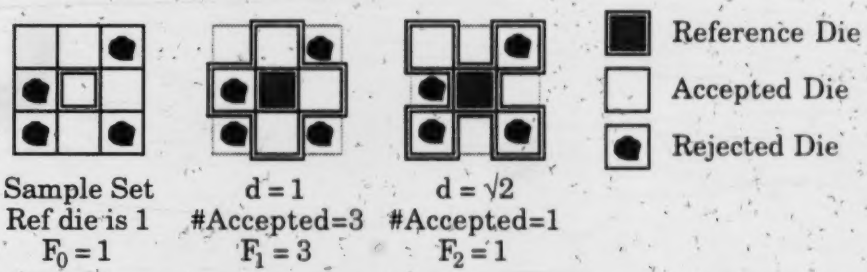


Figure 20. Calculation of proximity factors F_0, F_1 and F_2 for a sample pattern.

An Example of the 2-D Cluster Model

The use of the 2-D die proximity function may be demonstrated through a wafer with nine dies as shown in Figure 21. The illustration represents a wafer that has been tested by a set of compliance tests and four dies of the nine have been rejected.

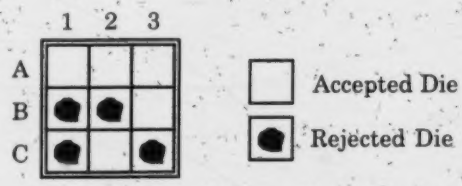


Figure 21. An example wafer with nine dies.

In this example only Set 1 and Set 2 will be used. The tabulating begins with the first die, A1, being chosen as the reference die. Since A1 is an accepted die, the proximity factor F_0 is 1. There is only one accepted die immediately adjacent to A1 (in Set 1), F_1 is equal to 1. In Set 2, there are no accepted dies, and F_2 is equal to 0. This is illustrated in Figure 22 (a).

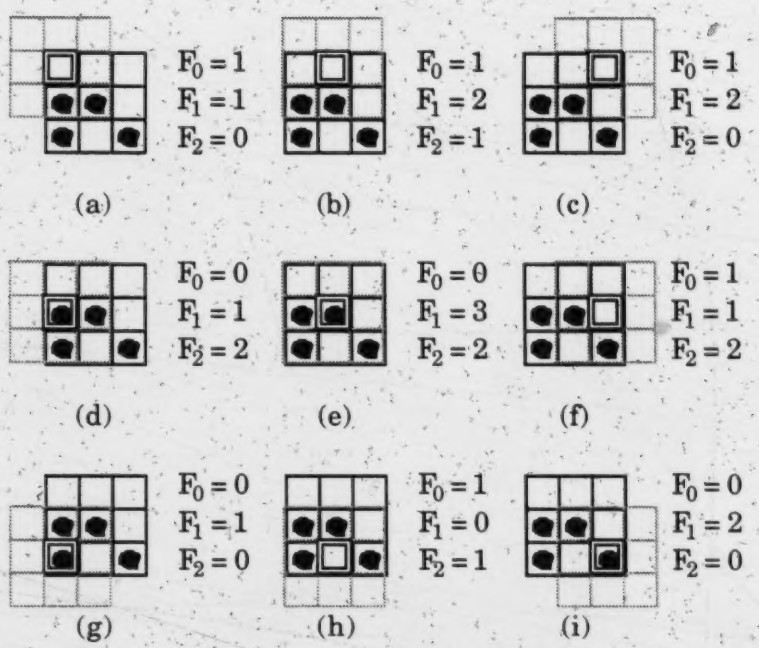


Figure 22. Determining proximity factors F_0, F_1, and F_2 (2-D)

As in the 1-D example, when the sets extend past the edge of the wafer, the 'dies' beyond the wafer are considered rejected dies and counted as zero. While this biases the calculations to represent a higher failure level at the edge, the number of accepted dies at the edge are usually fewer in number [17].

The next die, A2, is made the reference die as illustrated in Figure 22 (b), and the tabulation is repeated. The process continues with the rest of the dies on the wafer as illustrated in Figure 22 (c) to (i).

The results appear in Table 7.

Table 7. Proximity factor values for all the dies in the 2-D example.

Die	F_0	F_1	F_2
A1	1	1	0
A2	1	2	1
A3	1	2	0
B1	0	1	2
B2	0	3	2
B3	1	1	2
C1	0	1	0
C2	1	0	1
C3	0	2	0

As in the 1-D case, the cluster value is assigned to each die by weighting the proximity factors with a set of weighting coefficients. The form of the cluster equation is the same as before.

$$c_i = \varphi_0 F_0 + \varphi_1 F_1 + \varphi_2 F_2 + \varphi_3 F_3 + \ldots = \sum_{j=0}^{n} \varphi_j F_j \qquad (3)$$

where:

c_i - cluster value for the i^{th} die

φ_j - weighting coefficient for the j^{th} equidistant set

F_j - proximity factor for the j^{th} equidistant set

n - number of equidistant sets

For now, the coefficients φ_0, φ_1, φ_2 will be arbitrarily assigned the values 1, 0.75, and 0.25, respectively for illustration purposes only. Table 8 contains the proximity factors for each die and the cluster values based on the given weighting coefficients.

Table 8. Proximity factor and cluster values for the dies in the 2-D example.

Die	F_0	F_1	F_2	c_i
A1	1	1	0	1.75
A2	1	2	1	2.75
A3	1	2	0	2.50
B1	0	1	2	1.25
B2	0	3	2	2.75
B3	1	1	2	2.25
C1	0	1	0	0.75
C2	1	0	1	1.25
C3	0	2	0	1.50

The cluster values may be represented with a three dimensional bar chart. This is illustrated in Figure 23. The same bar chart with the data from the rejected dies removed clearly shows the difference in cluster values of the accepted dies.

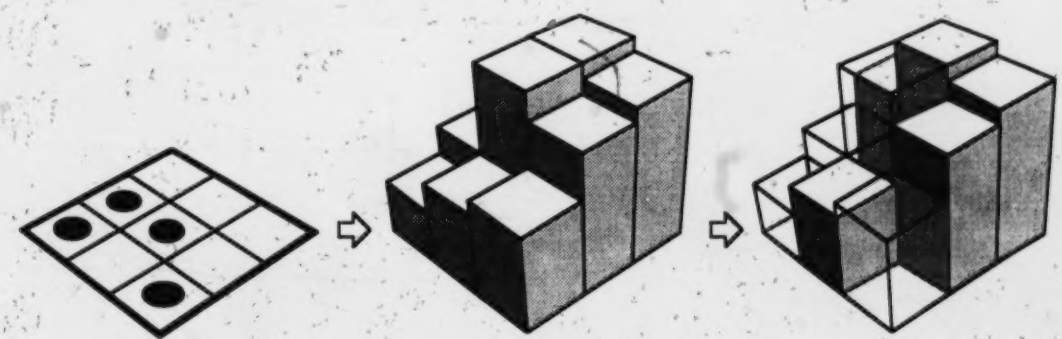


Figure 23. Transition from binary data to cluster values: (a) original binary data, (b) cluster values for all dies, (c) cluster values for accepted dies only.

As in the 1-D example, the cluster values reflect the pattern of die failure. When a die is situated among accepted dies, the cluster value will be high for that die. When a die is in a region of rejected dies, the cluster value

will be low. Again, the exact level of the cluster value for each die depends upon the values chosen for the weighting coefficients φ_0, φ_1, φ_2.

Overview of Analysis using Cluster Values for the 2-D Example

The dies in this example may now be analyzed with respect to their cluster values. The minimum acceptance level (MAL) is represented as a plane on the 3-D graph of cluster values. As in the 1-D example, the MAL may be adjusted depending upon the application. The resulting position of the plane dictates which dies will be further processed and which will be rejected or used for less demanding applications. In Figure 24, the MAL was set up for a hypothetical application. In this data set, all but one die are suitable for the application.

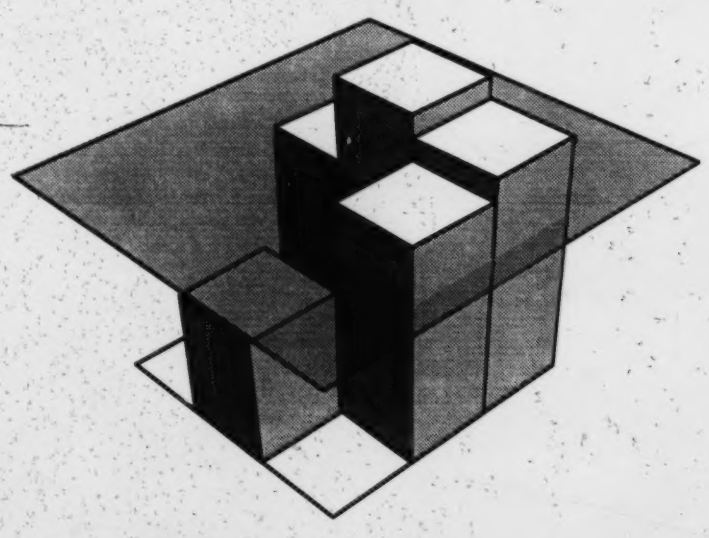


Figure 24. Example of a minimum acceptance plane set for a particular application requirement. Here one of the five accepted dies would not be accepted for use in the application environment.

Development of the 2-D Wafer Cluster Value

The 2-D wafer cluster value is produced by the addition of the cluster value of each die multiplied by the die's F_0 term. This is equivalent to the summation of the cluster values for only the accepted dies (whose F_0 values are 1). The form of the wafer cluster function for the k^{th} wafer is the same as in the 1-D example. This is shown in Equation 4 where N is the number of dies on the wafer.

$$wc_k = \sum_{i=1}^{N} F_{0i} \times c_i \qquad (4)$$

Again, the objective of the wafer cluster value is to reflect the level of dispersion or grouping of the accepted dies for a particular wafer. This enables wafers to be compared and ranked thus enabling the fabrication process to be evaluated over time.

INSIDE THE CLUSTER MODEL

Objectives of the Proximity Factor Weighting Coefficients

The weighting coefficients φ are picked to accomplish two objectives. First, the coefficients should weight the proximity factors appropriately to produce a unique die and wafer cluster value for each unique pattern of the accepted dies, i.e., two patterns should not by a matter of coincidence produce the same die and wafer values. Second, the range of cluster values should represent the range of patterns. That is, the die cluster value should be highest on a relative scale for an accepted die when it is

surrounded by accepted dies and lowest when an accepted die is surrounded by rejected dies. Similarly, the wafer cluster value should be highest on a relative scale for a wafer when it bears all accepted dies and lowest for a wafer when it bears all rejected dies.

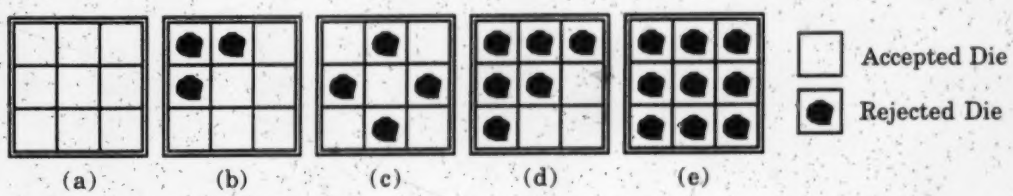


Figure 25. Examples of die failure clustering patterns.

The die and wafer cluster values should be highest for Figure 25 (a) and lowest for Figure 25 (e).

The following section presents the method used to determine the function to produce the φ weighting coefficients such that the die cluster value and the wafer cluster value meet the above constraints.

Determining a Function for the Weighting Coefficients

Two functions will be compared with respect to the φ weighting coefficients they produce for the proximity factors, F_0, F_1, F_2, F_3, F_4, and F_5. Only the first five equidistant sets have been chosen to keep computations manageable and yet obtain a significant level of variation between the results of the functions. The two functions that have been chosen for testing are the inverse distance function, and the Gaussian normal function.

The value for the i^{th} weighting coefficient is obtained from a given function by evaluating the function at a point representing the distance from a reference die to the i^{th} equidistant set. For example, Set 2 is the set of dies a distance $\sqrt{2}$ from the reference die. The weighting coefficient φ_2 will be the value of a given function evaluated at $\sqrt{2}$. This is demonstrated in Figure 26 with a sample function.

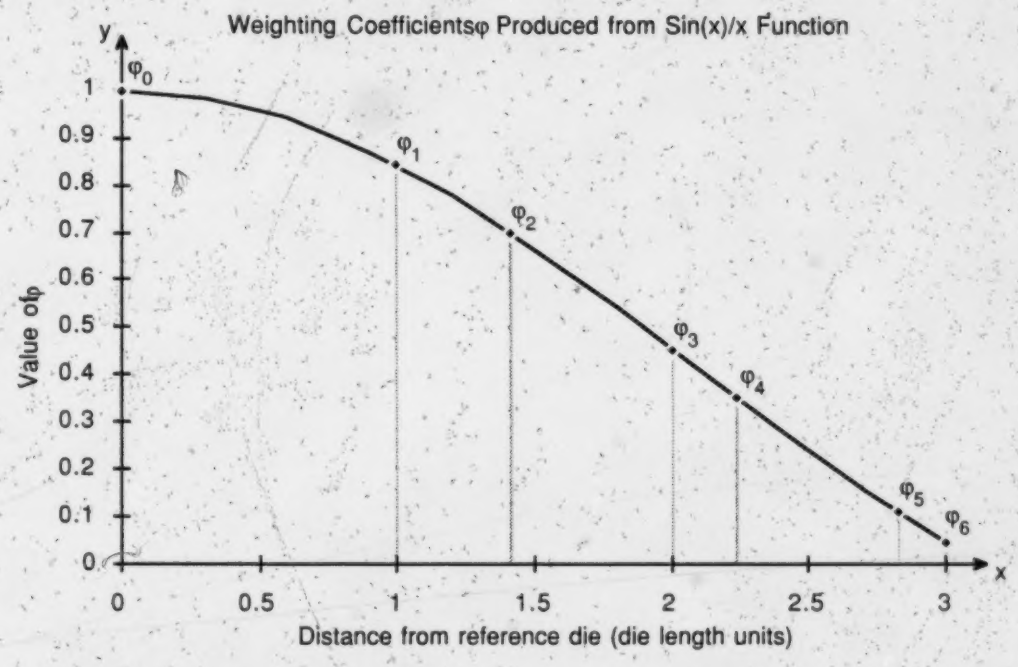


Figure 26. Weighting coefficients φ produced from Sin(x)/x function. The x value of each weighting coefficient φ is the distance used in its corresponding equidistant set (i.e., Set 1 d=1, Set 2 d=$\sqrt{2}$, Set 3 d=2, Set 4 d=$\sqrt{5}$, Set 5 d=$\sqrt{8}$, etc.). By evaluating a function at each corresponding distance produces a value for each φ.

The Inverse Distance Function

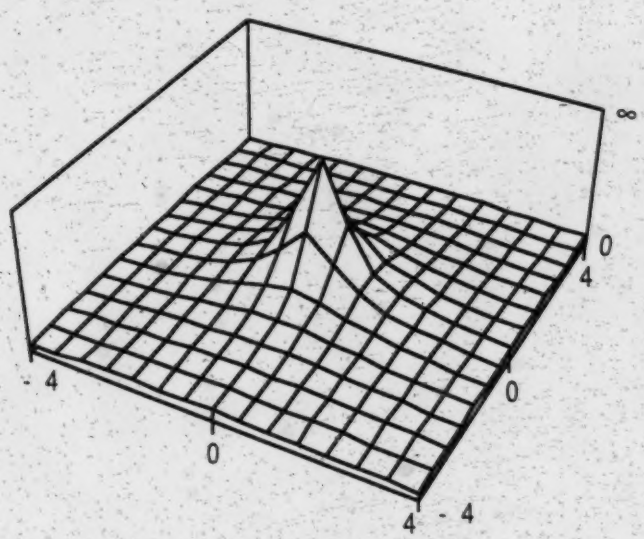


Figure 27. General form of the inverse distance function where the surface is defined by $f(x,y) = 1/\sqrt{(x^2 + y^2)}$.

The inverse distance function requires an adjustment at the origin since mathematically the value at that point is infinite. With $\varphi_0 = \infty$ the contributions from all proximity factors except F_0 become insignificant.

As shown in Figure 28, the value of three for the origin produces a suitable gentle curve. As a test, the cluster value equation was applied to a set of wafers with φ_0 set to 6, 12, and 18. Every set of cluster values produced was functionally equivalent to the cluster equation using $\varphi_0 = 3$ as a result of the weighting coefficient φ_0 dominating the equation. Hence, 3 was chosen for the value of φ_0.

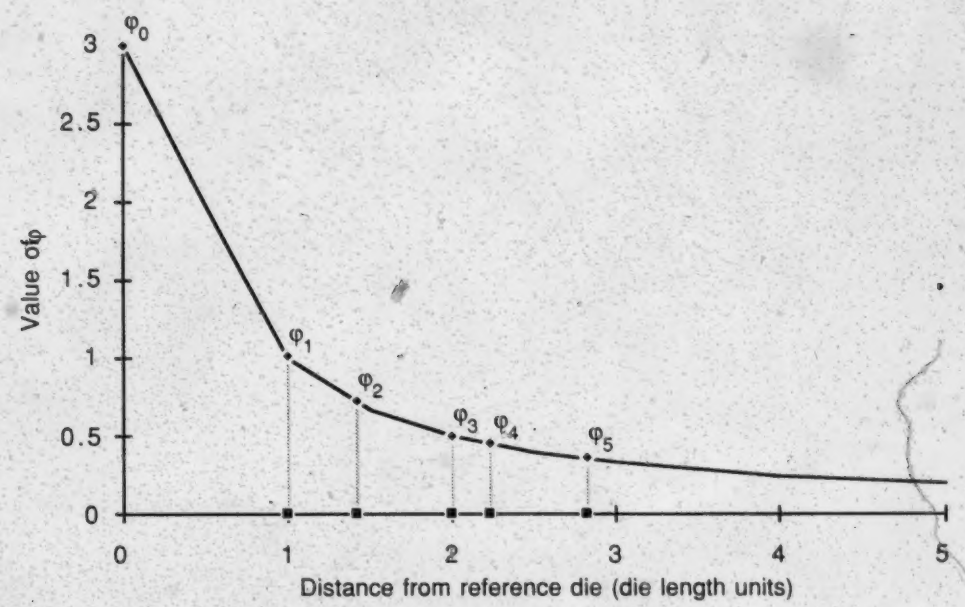


Figure 28. Special form of the inverse distance function used in the generation of weighting coefficients.

The weighting coefficients from the inverse function are, $\varphi_0 = 3$, $\varphi_1 = 1$, $\varphi_2 = 0.71$, $\varphi_3 = 0.50$, $\varphi_4 = 0.45$, and $\varphi_5 = 0.35$. Thus the equation for the cluster value becomes Equation 5.

$$c_i = 3*F_0 + 1*F_1 + 0.70710678*F_2 + 0.5*F_3 + 0.4472136*F_4 + 0.35355339*F_5 \quad (5)$$

The Gaussian Function

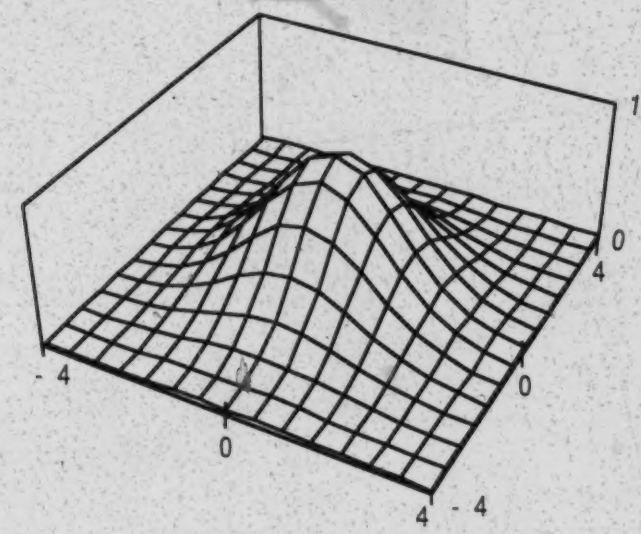


Figure 29. General form of the Gaussian function where the surface is defined by Equation 6.

While the Gaussian function (defined by Equation 6) and its associated parameters, the population standard deviation σ and the population mean μ, are usually used in a statistical context, the cluster model uses the function simply as a mathematical function to generate the weighting coefficients.

$$f(x; \mu, \sigma^2) = \frac{1}{\sqrt{2\pi}\,\sigma} e^{-\frac{1}{2}\left(\frac{x-\mu}{\sigma}\right)^2} \qquad (6)$$

The parameter σ will be used to control the shape of the Gaussian function as shown in Figure 30. The parameter μ is set to zero since the function will always be centred over the reference die. The parameter x is defined as the distance between die centres in die length units.

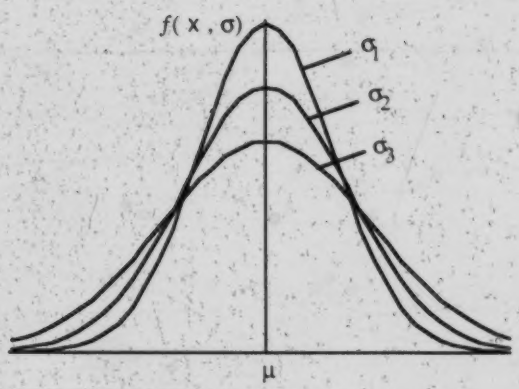


Figure 30. Control of the Gaussian function shape through modification of parameter σ.

Since only proximity factors up to F_5 are of interest, the shape of the Gaussian function is set such that proximity factors F_6 and higher, if they were to be included, would not contribute significantly to the cluster value.

It was found that if the weighting coefficient for F_6 was set to 1/10 the value of the weighting coefficient for F_0, this requirement would be achieved. The value of σ required to set this shape is 1.39797181. This corresponds to the function shown in Figure 31.

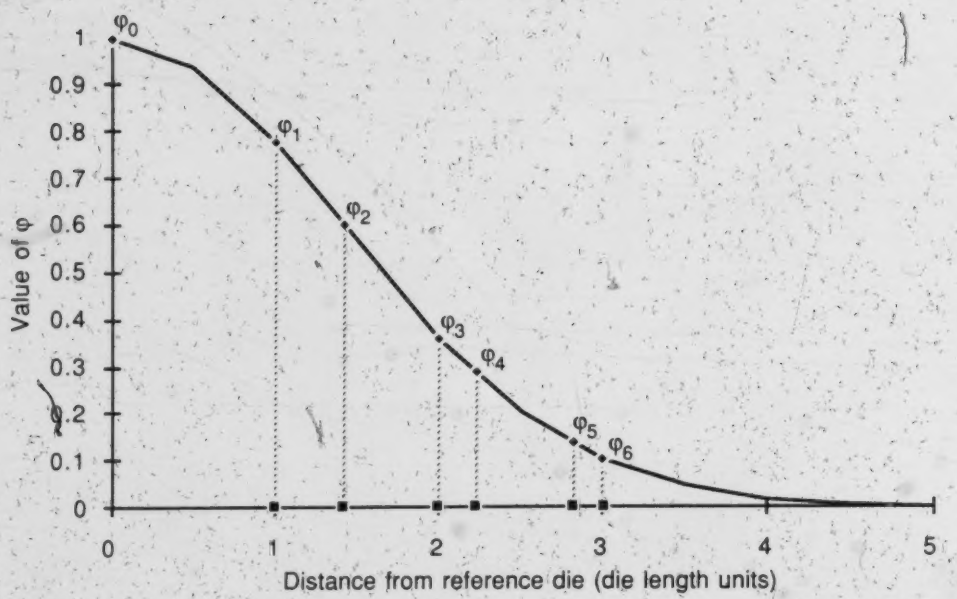


Figure 31. Gaussian function using $\sigma = 1.40$ with the curve scaled to set the maximum height to one. Note that the value of φ_6 (for dies 3 units away) is one tenth of the value of φ_0.

The weighting coefficients for this function are $\varphi_0 = 1.00$, $\varphi_1 = 0.77$, $\varphi_2 = 0.60$, $\varphi_3 = 0.36$, $\varphi_4 = 0.28$, and $\varphi_5 = 0.13$. The cluster equation using this set of coefficients becomes Equation 7.

$$c_i = 1*F_0 + 0.77426368*F_1 + 0.59948425*F_2 + 0.35938137*F_3 + 0.27825594*F_4 + 0.12915497*F_5 \quad (7)$$

Test Set for the Evaluation of the Functions

To formulate a basis for comparing the functions, test wafers of 3×3 dies were generated using binary sequence encoding. With 9 accepted or rejected dies arranged in a 3×3 pattern, there are 512 (2^9) possible die patterns. Using binary sequence encoding, each sequential number from 0 to 511 is transformed into a die pattern by converting the number into a

nine digit binary equivalent. The binary number is mapped onto the 3×3 grid using the exponents of 2 which are mapped out beginning with the lower right corner of the grid. For example, wafer 98 has the die pattern shown in Figure 32.

$$98 = 0\times2^8 + 0\times2^7 + 0\times2^6 + 0\times2^5 + 0\times2^4 + 0\times2^3 + 0\times2^2 + 0\times2^1 + 0\times2^0 = 001100010_2$$

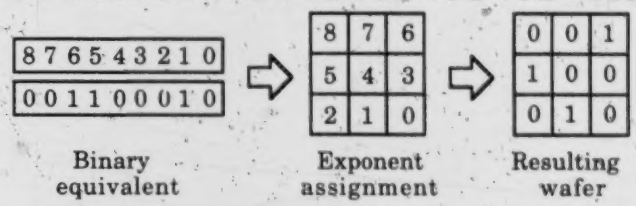


Figure 32. The creation of a test set using the wafer number to generate a unique die layout. The wafer number is converted into a 9 digit binary representation which is transposed onto the 3×3 grid.

A table of proximity factors (shown in Appendix Table A3), from F_0 to F_5, was constructed from the patterns on the 512 wafers using the first five equidistant sets. The analysis of wafer 96 is shown in Figure 33.

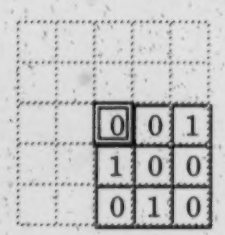


Figure 33. Analyzing of the first cell of wafer 98 to obtain the corresponding set of proximity factors. The dies past the wafer edge are considered rejected or '0'.

A portion of the proximity factor table is shown in Table 9 for the patterns shown in Figure 34.

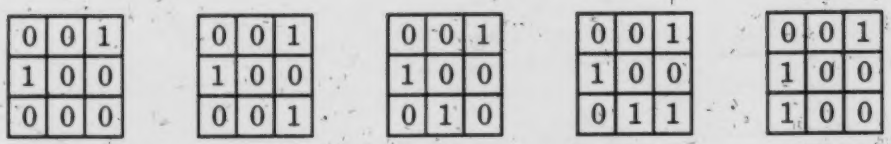


Figure 34. A sample of the set of die patterns used.

The complete list of proximity factors is found in Appendix Table (A3).

Table 9. A portion of the factor table for the 512 test wafers (from Appendix Table A3). Wafer proximity factors are simply the sum of all individual die proximity factors.

Wafer Number	F_0	F_1	F_2	F_3	F_4	F_5
96	2	0	0	0	2	0
97	3	0	0	2	4	0
98	3	0	2	0	4	0
99	4	2	2	2	6	0
100	3	2	0	0	2	2

Since patterns with the same values of proximity factors will have the same wafer cluster value, it is possible to increase the efficiency of the evaluation by discarding those wafers with equivalent proximity factors. Duplicate proximity factor table entries result from graphical pattern manipulations of a wafer die pattern. The possible manipulations are orthogonal rotation, mirroring, and cell shifts. For instance, wafer 98 has a proximity factor table entry of {3 0 2 0 4 0}. Progressive rotation and mirroring of this wafer, as shown in Figure 35, produces other wafers with the same relative pattern and the same proximity factor values.

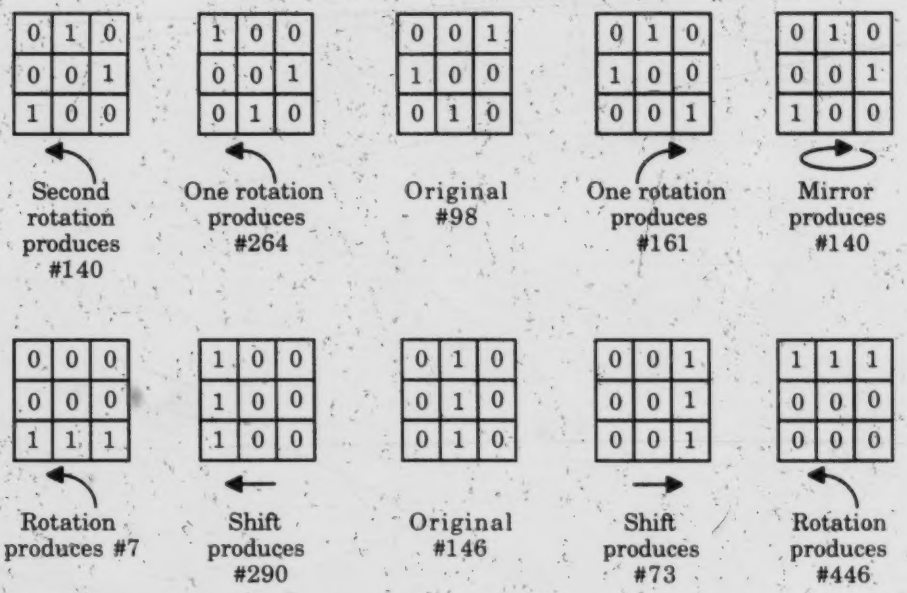


Figure 35. Proximity factor and pattern equivalent wafers determined from pattern manipulations.

With the duplicates removed, 86 unique wafers out of the original 512 and their corresponding unique proximity factor values are retained. This represents an 83% reduction in the test set and consequently in the computational requirements.

Comparison Method

The maximum cluster value produced by the two functions differed greatly as did the increments in the cluster values of successive test wafers. To form a basis for comparison, the following method was used. The 86 test wafers were arranged in order of the cluster values produced by the Inverse Distance function. Each wafer was assigned an ordinal value from 1 to 86 indicating its position in the sort order. The test wafers were then resorted using the Gaussian function. The wafers were

assigned a second set of ordinal values. These two ordinal lists were used to compare the results of the two functions. The sort order for each function is given in Appendix Table A3, with a portion reproduced in Table 10.

Table 10. A portion of the data for the 86 test wafers showing the proximity factor values, the calculated cluster values and the order of the wafers when sorted on each of the two sets of cluster values (from Appendix Table A3).

Test							Cluster Values		Sort Order	
Wafer	F0	F1	F2	F3	F4	F5	Inv.	Gau.	Inv.	Gau.
0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	3	1	2	2
3	2	2	0	0	0	0	8	3.549	7	7
5	2	0	0	2	0	0	7	2.719	5	5
7	3	4	0	2	0	0	14	6.816	16	16
10	2	0	2	0	0	0	7.414	3.199	6	6
11	3	4	2	0	0	0	14.414	7.296	17	17
...			...				...	...	...	
95	6	12	8	4	4	2	40.153	22.896	71	71
97	3	0	0	2	4	0	11.789	4.832	9	9
98	3	0	2	0	4	0	12.203	5.312	10	10
99	4	2	2	2	6	0	19.097	9.136	21	20
101	4	2	0	4	4	2	18.496	8.357	19	19
102	4	4	2	0	4	2	19.910	9.667	30	27
...			...				...	...	...	
365	6	8	0	10	8	4	35.992	18.531	59	59
367	7	12	4	10	12	4	47.609	26.139	75	75
381	7	12	8	10	8	4	48.649	27.424	76	76
383	8	18	12	10	12	4	62.266	36.580	84	84
495	8	16	8	12	16	4	60.226	34.465	83	83
511	9	24	16	12	16	4	76.883	46.455	86	86

The sort order indicates each function's ordering of the test wafers from the least clustered accepted die patterns to the most clustered accepted die patterns. The graph in Figure 36 shows the similarity in sort order between the two functions. This graph uses the last two columns of Table

10 with test wafers sorted in the order of Inverse Distance which therefore appears as a straight line.

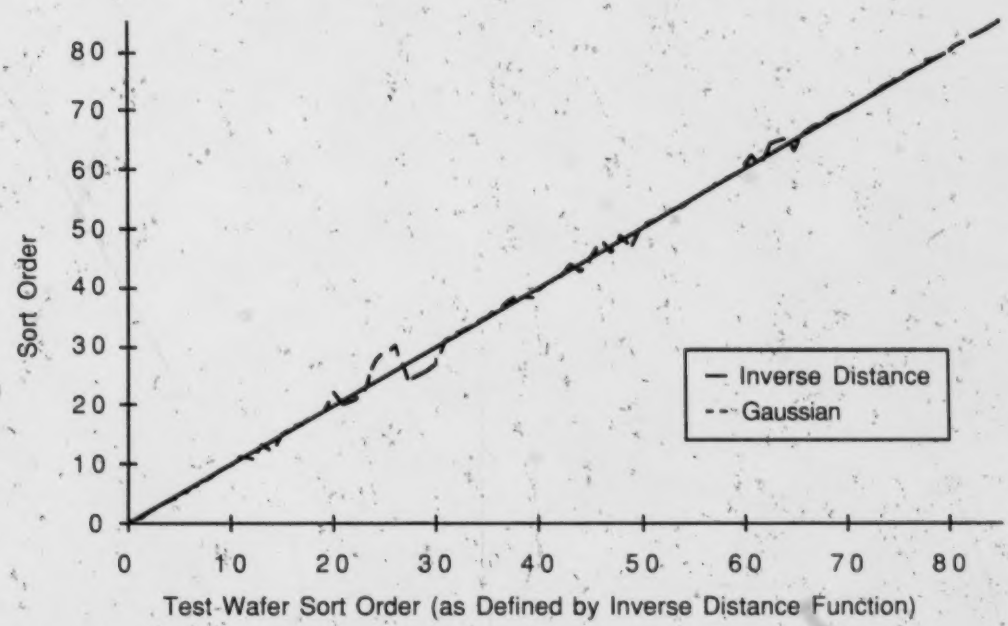


Figure 36. Inverse Distance and Gaussian sort list in the order specified by the Inverse Distance function.

To determine which function produced the best ordering of the test wafers, the wafers with the most disagreement in sort order were examined. Figure 37 is an enlarged section of the above graph showing the order of the 20th to 30th test wafers.

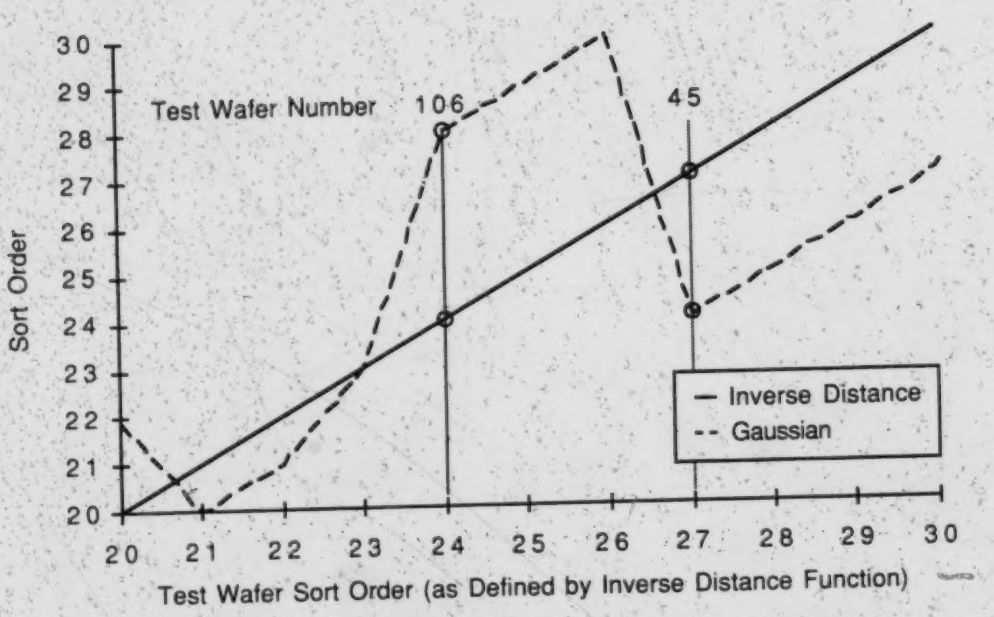
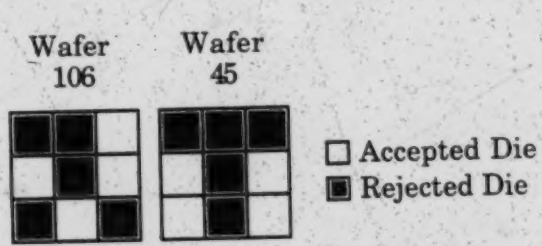


Figure 37. Enlarged view of the sort order based on Inverse Distance. The 24th and 27th test wafers (wafer numbers 106 and 45) are sorted by the Gaussian function as the 28th and 24th wafers.

The 24th and 27th test wafers (wafer numbers 106, and 45) were compared since the two functions differed greatly in the ordering of the two. Figure 38 shows the two test wafers with the proximity factor table entries.



F(106) = {4 2 4 2 4 0}
F(45) = {4 4 0 4 4 0}

Figure 38. Test wafer patterns 106 and 45, and the corresponding proximity factors.

From the list of proximity factors, both wafers have the same number of accepted dies (from F_0). Wafer 45 has a larger F_1 proximity factor than wafer 106 which indicates that more of the dies are immediately adjacent (in this case, 1 set of dies more). However, wafer 106 has a significantly higher F_2 factor which indicates that more of the dies are corner adjacent (in this case, 2 sets of dies more). The sort order for these two is highly dependent upon the weighting assigned to the proximity factors.

To solve the dilemma in order the wafers should be placed, the wafers can be examined in terms of the clustering patterns of the rejected dies. Wafers with high clustering of accepted dies should also have a correspondingly low clustering of rejected dies. The wafer cluster value for rejected dies, wc_{Rk}, is calculated through the addition of the cluster values for the rejected dies. Mathematically, this is performed by multiplying the cluster value of each die, c_i, with the complement of the yield for the individual die, equivalent to $(1 - F_{0i})$, as shown in Equation 8.

$$wc_{Rk} = \sum_{i=1}^{N} \overline{F_{0i}} \times c_i \qquad (8)$$

The layout with the greatest clustering of rejected dies should be considered lower in the accepted sort order. Wafer 106 has a rejected proximity factor list of F(106) = { 5 4 6 4 4 2 }, and wafer 45 has a rejected proximity factor list of F(45) = { 5 8 4 4 4 0 }. Wafer 45 has a larger F_1 proximity factor than wafer 106 which indicates that more of the dies are immediately adjacent (in this case, 2 set of dies more). Wafer 45 has a

smaller F_2 proximity factor indicating 1 set fewer of dies that are corner adjacent.

As a result, wafer 45 has the greatest clustering of rejected dies. Therefore, it should be lower in the sort order. This is the sort order suggested by the Gaussian function. Other examinations of wafer sort order differences produce the same results: the Gaussian function produces the most "correct" sort order or comparison method between wafers. It is suggested that the Gaussian function with $\sigma = 1.39797181$ should be used as a starting point in the analysis of wafers.

Future Directions

The difference between the two functions above is the weighting of the five proximity factors. As can be seen from the above example, even subtle differences in the coefficient weighting will produce variations in the manner wafers are sorted. Thus, a possible future enhancement to the cluster model is one where the coefficient weighting changes over the yield range from 0% to 100%. Consider Figure 39.

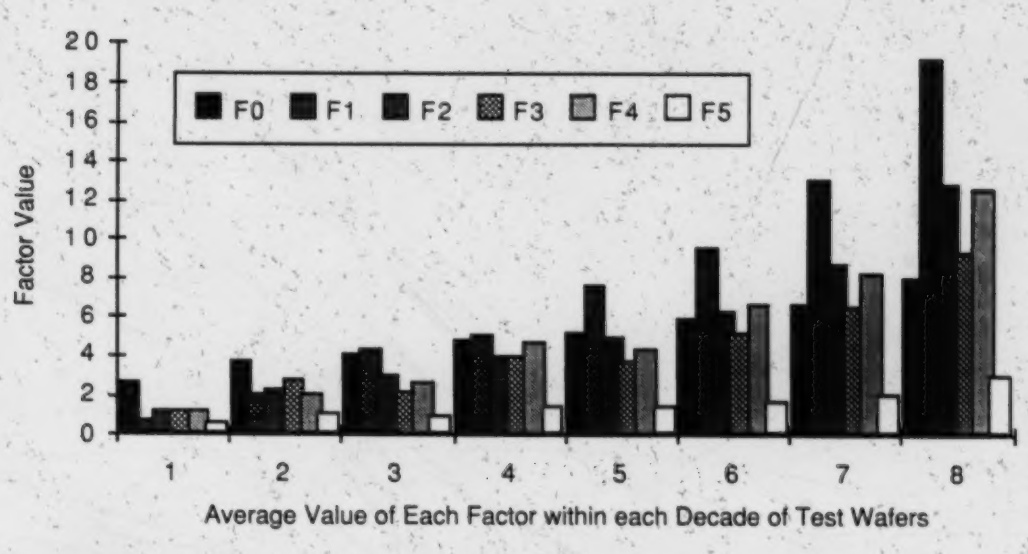


Figure 39. Relative contribution of each proximity factor to the cluster value as the yield for the 86 data wafers changes from 0% to 100%.

Figure 39 not only shows the rise in the cluster value as yield increases but also that the proximity factors increase at different rates. Through empirical studies, it may be possible to represent the weighting coefficient as a function rather than as a constant.

CHAPTER 4

COMPARISON OF THE CLUSTER MODEL TO INDUSTRIAL MODELS

THE OBJECTIVES OF EXISTING MODELS

This section compares the objectives and the results of industry accepted models for yield to those of the proposed cluster model. Before examining the objectives of the various models, the following question is raised: "Why do researchers model yield?" The generally accepted answer is to understand the factors that affect yield and by doing so provide an insight how these factors may be controlled to produce the highest level of yield. Ultimately, the exact form of this answer will depend on the objectives of the individual researcher and the objectives of their facility.

In this thesis, the second part of this answer, how factors may be controlled to produce the highest level of yield, is here considered the more important of the two parts. Unless the research into yield in some way produces procedures and algorithms for improving manufacturing lines, the research becomes an end in itself. In current literature [19-23], various authors attempt to understand the processes that control yield through researching various mathematical models based on forms such as compound Poisson, negative binomial, or Neymann Type A. However, the method of applying the results of the models to improving yield in the fabrication line in their works is implied but not implemented.

On the other hand, methods put forth by companies such as Enhansys Inc. [14], and authors such as Casper and Soren [18], provide practical approaches that are directly applicable.

THE OBJECTIVES OF THE CLUSTER MODEL

The cluster model, unlike currently existing models that provide methods for yield prediction, provides a yield analysis method [19]. At the end of the wafer acceptance stage, the cluster model provides information about the accepted dies to permit decisions to be made about further processing. Using the values that are generated from the model, it is possible to sort dies by their proximity to clusters of accepted dies. This proximity may be shown, with further empirical studies, to have a possible correlation to the reliability of the die. Thus, dies that are not part of, or close to, clusters of accepted dies may be removed from further processing as a cost saving measure. The model also facilitates automatic analysis and sorting of wafers and dies since these processing decisions may be made a part of the regular testing and sorting procedures.

MODELS BASED ON RANDOMLY DISTRIBUTED POINT DEFECTS

It is commonly considered that many of the causes of die failure mechanisms, referred to here as faults, are random in nature [20]. Assuming this is the case, these faults could be modeled through mathematical functions that describe random events. The most commonly used function in industry is the Poisson distribution.

Analysis of Poisson distribution for modeling point defects

In this section, the premises of the Poisson distribution are analyzed to evaluate its effectiveness to predict yield from fabrication data.

The following terms will be used:

n - the number of point defects per wafer

N - the number of dies on a wafer

p - the probability that a die contains point defects

q - probability that a die contains no point defects

Other terms will be defined as required.

If **n** point defects are randomly distributed among **N** dies on a wafer, then each die on the wafer is equally susceptible to point defects. The number of point defects per die can vary from 0 to **n** point defects about the mean number of point defects per die. This variation in the number of point defects per die can be described by a binomial distribution characterized by two parameters, namely **p** and **n**, where **n** is the number of point defects per wafer and **p** is the probability that an individual die contains point defects. The probability **q** that a die contains no point defects is calculated as follows:

$$q = 1 - p \tag{9}$$

Each term in the expansion of the binomial distribution represents the probability that an individual die contains a certain number of point defects. The terms of the binomial distribution are shown in Equation (10).

$$(p + q)^n = p^0 + nC_1\, p^1\, q^{n-1} + nC_2\, p^2\, q^{n-2} + \ldots$$

$$+ nC_k\, p^k\, q^{n-k} + \ldots + nC_n\, p^n \qquad (10)$$

where: p^0 - probability that a die contains 0 point defects

nC_1, nC_2, nC_k - binomial coefficients

$nC_1\, p^1\, q^{n-1}$ - probability that a die contains 1 point defect

$nC_2\, p^2\, q^{n-2}$ - probability that a die contains 2 point defects

$nC_k\, p^k\, q^{n-k}$ - probability that a die contains **k** point defects

$nC_n\, p^n$ - probability that a die contains **n** point defects

The probability that a die contains **k** point defects is the k^{th} term of the expansion.

$$P(k) = nC_k\, p^k\, q^{n-k} \qquad (11)$$

Each die on a wafer has an equal probability of containing point defects based on the precondition that the point defects are uniformly distributed among the **N** dies on the wafer. Therefore, the probability **p** that an individual die contains point defects is,

$$p = 1/N \qquad (12)$$

The probability **q** that a die contains no point defects is,

$$q = 1 - p = 1 - (1/N) = (N-1)/N \qquad (13)$$

Equation 11 can be rewritten to include equations 12 and 13 as follows:

$$P(k) = nC_k\, (1/N)^k\, ((N-1)/N)^{n-k}$$

$$= nC_k \frac{(N-1)^{n-k}}{N^n} \qquad (14)$$

The yield of a die (the condition **k=0**) can be estimated as follows:

$$P(0) = \frac{(N-1)^n}{N^n} \tag{15}$$

The expected number of dies on a wafer that have no defects is,

$$E(N_0) = P(0) \times N \tag{16}$$

where: N_0 - number of dies on a wafer with no defects

The yield, **Y**, for a given wafer is defined by the following expression:

$$\begin{aligned} Y &= \frac{\textbf{number of dies with no point defects}}{\textbf{total number of dies on the wafer}} \\ &= E(N_0)/N \\ &= P(0) \end{aligned} \tag{17}$$

If the number of defects **n** per wafer is significantly greater than the number of defects per die **k** (**n >> k**), then the following terms in the binomial expression, **P(k)**, can be simplified as follows:

$$\begin{aligned} {}_nC_k = \frac{n!}{(n-k)!} &= \frac{(n)\,(n-1)\,(n-2)\,\ldots\,(n-k)\,(n-k-1)\,(n-k-2)\,\ldots}{(n-k)\,(n-k-1)\,(n-k-2)\,\ldots} \\ &= (n)\,(n-1)\,(n-2)\,\ldots\,(n-k+1) \\ &\approx n^k \end{aligned}$$

$$\frac{(N-1)^{n-k}}{N^n} = \frac{1}{N^k}\,\frac{(N-1)^{n-k}}{(N)^{n-k}} \approx \frac{1}{N^k}\,(1 - 1/N)^n \tag{18}$$

The term $(1 - 1/N)^n$ can be expanded into the following series:

$$1 - \frac{n}{N} + \frac{n(n-1)\,(1/N)^2}{2!} - \frac{n(n-1)(n-2)\,(1/N)^3}{3!} + \ldots \tag{19}$$

If the term **n** is very large (the condition **(n-1)** ≈ **n**), the above expression can be approximated as follows:

$$1 - n/N + \frac{(n/N)^2}{2!} - \frac{(n/N)^3}{3!} + \ldots \qquad (20)$$

The above MacLaurin expression is equivalent to the following exponential function:

$$e^{-n/N} = 1 - n/N + (n/N)^2 - (n/N)^3 + \ldots$$
$$= e^{-m} \qquad (21)$$

where: $m = n/N$

Rewriting the binomial expression for **P(k)** with the above approximations produces the following Poisson distribution:

$$P(k) = \frac{n^k}{N^k} \frac{e^{-m}}{k!} = \frac{m^k}{k!} e^{-m} \qquad (22)$$

The primary question, then, concerning the Poisson representation of the wafer failure process is, "How accurate does the Poisson probability distribution represent the binomial distribution?"

If (and only if) the point defects are randomly distributed over the entire surface of the wafer, can the Poisson distribution parameters (representing an estimate of a wafer's yield) be modified to be functionally dependent upon the area of a die, **A**, and the number of wafer defects per unit die area, $D_o = n/NA$ (where **N** is the number of dies per wafer). If the average number of point defects per die is given by $m = n/N$, then **m** may be represented as in Equation 23.

$$m = \frac{n}{N} = \frac{DoNA}{N} = DoA \tag{23}$$

Then P(k) may be expressed as Equation 24.

$$P(k) = \frac{m^k}{k!} e^{-m} = \frac{(DoA)^k}{k!} e^{-DoA} \tag{24}$$

The yield of a wafer (the condition **k=0**) is equal to:

$$P(k=0) = YIELD = e^{-DoA} = e^{-m} \tag{25}$$

It is clear from Table 11 that as the number of defects per wafer, **n**, increases, the error in the Poisson model results increases significantly.

Table 11. Comparison of the Poisson model of yield to the binomial model based on two sample sets of wafers, one wafer with 3 dies and one with 4 dies.

		YIELD		
N	n	POISSON MODEL	BINOMIAL MODEL	% ERROR
3	1	0.716531311	0.666666	7.48
3	2	0.513417119	0.444444	15.52
3	3	0.367879441	0.296296	24.16
4	1	0.778800783	0.75	3.84
4	2	0.606543066	0.5625	7.83
4	3	0.472366553	0.421875	11.97
4	4	0.367879441	0.31640625	16.27

If the average number of defects per die, **m**, is small (less than 0.33), then the Poisson model provides a good estimate of the binomial failure model. As a result, the Poisson model should be limited to the analysis of high yield wafers only.

Modifications to the Poisson distribution

It is generally accepted that the Poisson distribution is not an adequate model of yield if the defect density is high. To use the Poisson distribution in these circumstances, researchers have modified the distribution using partitioning [20, 21], or region density calculations.

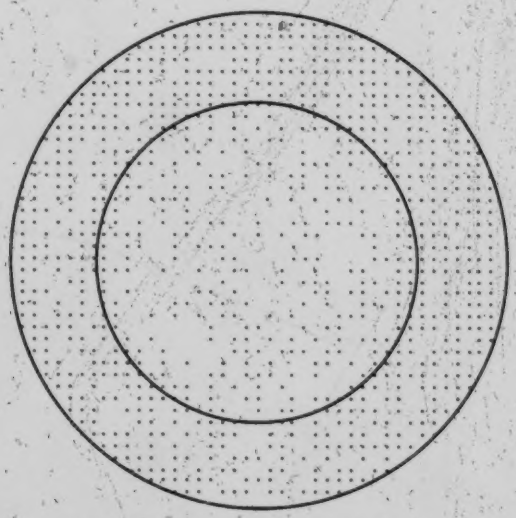


Figure 40. An example of partitioning two distinct theoretical zones of defect density on a wafer.

In actual practice, the contours that would be required to properly zone the various defect densities would be more of the order of Figure 41.

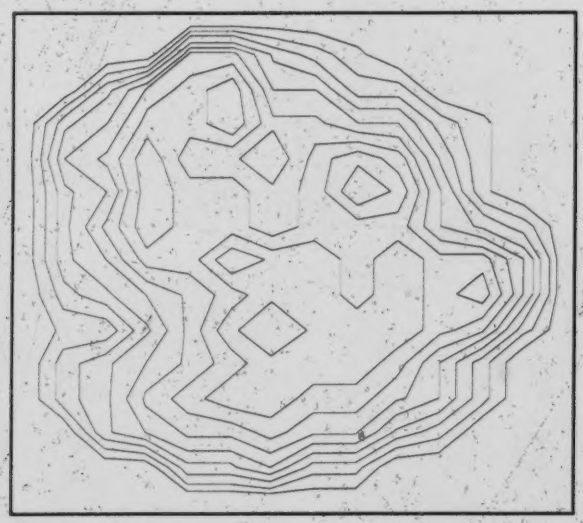
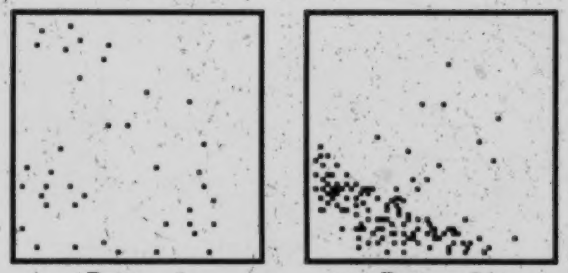


Figure 41. Yield contour based on a sample wafer's die failure pattern. [based on research performed by author]

This diagram was formed from a die failure pattern with the contours indicating the relative pattern of accepted dies to rejected dies. As shown in the previous section, modeling yield with the Poisson distribution produces significant errors when the defect density is high. In addition, it has been shown by Petritz [22] that Poisson modeling of yield is pessimistic if the defects are clustered or grouped.

In either case, it becomes prudent to test the data to ensure that it is randomly distributed over the area of interest.

In Figure 42, two particle patterns are shown that were included in an analysis using the Poisson distribution [8].



Pattern 1 Pattern 8

Figure 42. Particle maps obtained with an electronic particle detector.

In the reference, the patterns were partitioned into a grid of 6×6 cells, and the number of defects in each cell was recorded.

2	3	1	0	0	0
0	1	1	1	0	0
0	0	2	0	1	0
2	1	0	1	2	0
4	3	0	0	3	0
2	1	2	2	4	0

Pattern 1

0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	1	1	0
6	1	1	1	2	0
28	20	10	0	0	0
1	20	22	19	4	1

Pattern 8

Figure 43. Particle counts from a grid analysis of patterns 1 and 8 Each number represents the number of particles found in each cell.

For pattern 1, the frequency of particles per cell is graphed in Figure 44 with the theoretical expected values E(x) obtained using the Poisson distribution.

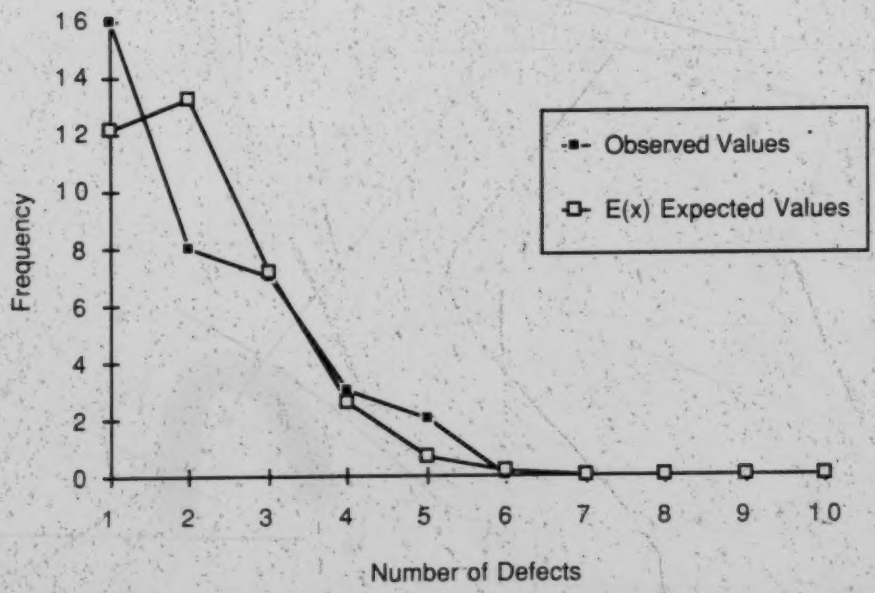


Figure 44. The observed frequency of defects per cell superimposed upon the calculated expected values for pattern 1.

Visually, the observed and expected values correspond to one another. As a validation of the fit, the χ^2 value for pattern 1 was calculated. In this case, there are two degrees of freedom using the rule of combining data such that no E(x) is less than 5. The χ^2 value was determined to be 4.3657. This is below the χ^2 value of 5.991 (using a significance of α=0.05). The pattern, then, is acceptable as data for a Poisson distribution, and a simulation should produce reasonable results.

In a similar fashion, the frequency of defects per cell for pattern 8 is graphed in Figure 45, with the theoretical expected value E(x).

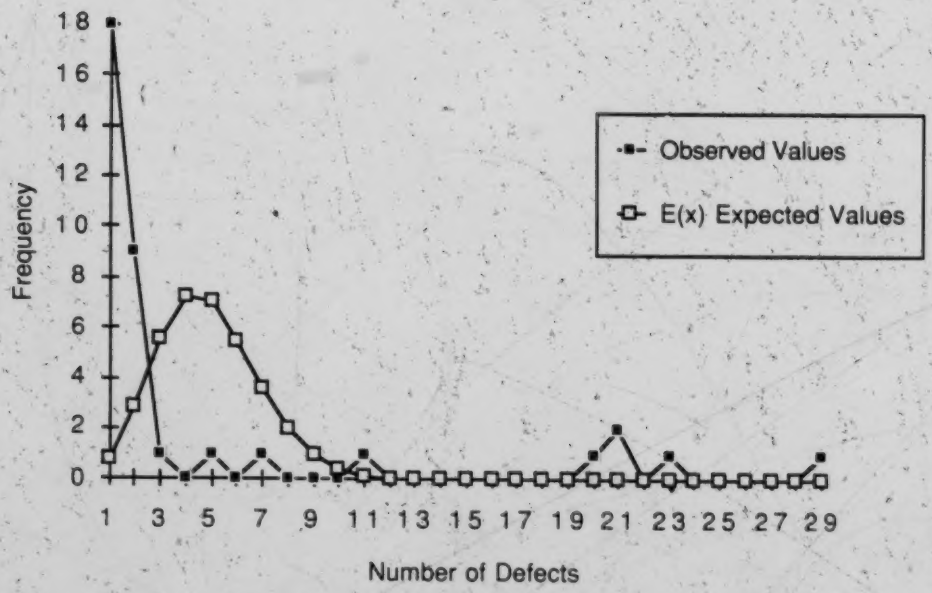


Figure 45. The observed frequency of defects per cell and the calculated expected values for pattern 8.

Visually, the observed and expected values do not correspond well to each other for this defect pattern. This is to be expected due to the high number of defects found in some cells. In this case, there are four degrees of freedom (using the rule of combining data such that no E(x) is less than 5), and thus the χ^2 value must be below 9.488. The χ^2 value for pattern 8 was calculated to be approximately 56, well above 9.488, and as such a Poisson distribution would not provide a good fit.

The level of defects and the clustering of defects do not affect the cluster model since it uses the die yield as data and hence is not subject to the restrictions of the Poisson modeling method.

Numeric Vertical Yield Mapping

As stated previously, the cluster model was designed as a yield analysis method. Current yield analysis methods begin by combining the die yields for the same die location over a group of wafers as shown in Figure 46.

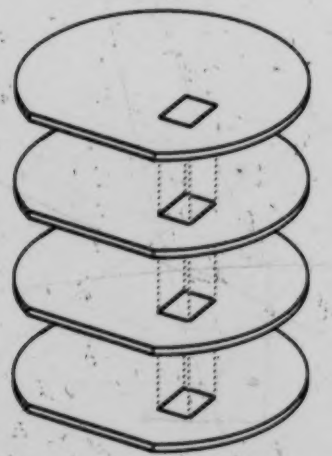


Figure 46. Vertical yield maps are generated by totaling the number of die yields for each die location over an entire set of wafers. [23]

This produces a combined yield map as shown in Figure 47.

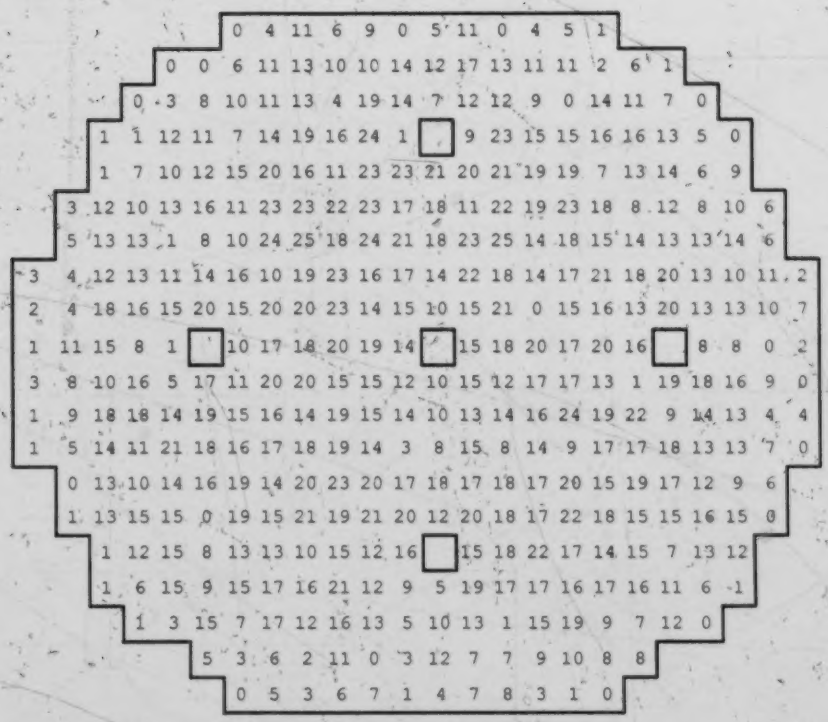


Figure 47. Numeric vertical yield map for 35 wafers [23]. The blank squares are the locations of the process monitors.

This data is shown as a three dimensional graphic in Figure 48.

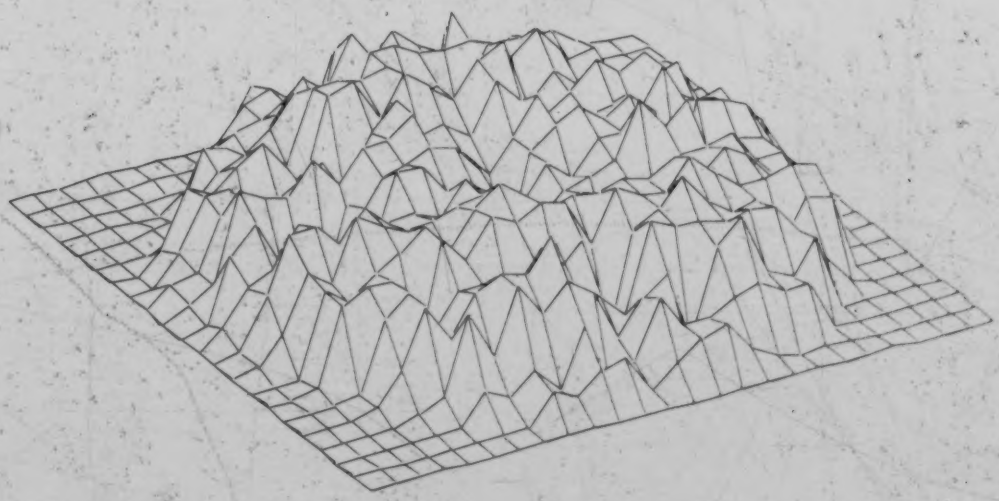


Figure 48. Surface rendering of the data in the vertical yield map for 35 wafers.

Visually, the pattern in Figure 48 is very complex, which suggests that many defect processes are acting upon the wafer group. This may be a result of extrinsic factors such as the fabrication process varying with time, or intrinsic factors such as wafer crystal and resistivity variations. In either case, this method produces a database that is extremely difficult to divide into its individual components.

As a result, a limitation of the numeric vertical yield method is an insensitivity to sudden changes in the fabrication process. Any variations that occur in the process, become masked by the rest of the data in the set. While the method can show the gradual changes in the process by comparing the analysis for wafer sets at different points in time, it cannot provide an indication of trend from one wafer to the next.

As well, this method assumes that failure patterns are aligned to the alignment flat of the wafer. Those that are, would arise from the processing equipment which handles each wafer in the same orientation. However, wafer resistivity, particulate contamination, and many other contributors to die failures are insensitive to the alignment flat, and as a result, are insensitive to the orientation of a wafer.

By concentrating on one wafer at a time, the cluster model provides a structure within which to analyze the processes that have affected each wafer individually. If the patterns of the process vary from one wafer to the next (as the unique die failure patterns on each wafer would suggest), any information conveyed in the patterns would be lost upon combining with data from other wafers.

CHAPTER 5

APPLICABILITY TO RELIABILITY ENGINEERING AND FABRICATION LINES

INTRODUCTION

The design of the cluster model allows it to be easily introduced into a fabrication line. Since ATE (automatic test equipment) use microprocessors, the additional code to calculate the cluster value for each die can easily be implemented. With the code in place, the ATE can generate reports of the die and wafer cluster values thus enabling the process modifications as outlined in this section.

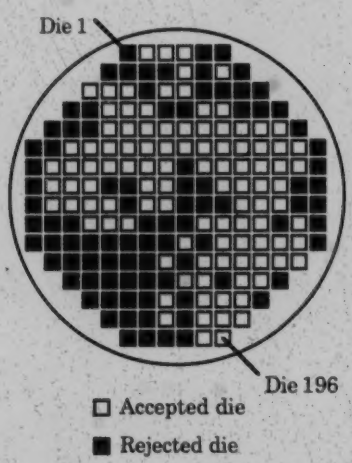
COST SAVING MEASURES

The cluster method may be used by manufacturers as a cost saving measure. The screening of accepted dies that have a high probability of failing in later quality control tests allows the saving of packaging, processing, and testing costs. These accepted dies will be referred to as "marginal" dies, indicating that although passed by the ATE, normal operating conditions could cause them to fail. Identifying the dies as early as possible in the manufacturing process eliminates the expense of bonding, encapsulation, and the associated quality controls. If burn-in tests are usually performed, even greater savings could be realized.

Pre-encapsulation testing for marginal dies

The cluster value for each die indicates its proximity to other accepted and rejected dies. The lower the cluster value for an accepted die, the closer is its position to an area of rejected dies. If any of the die failure mechanisms extend past the edges of the rejected dies, the accepted dies close by could be affected. Such dies could be marginal since the failure mechanisms that resulted in rejected dies may be latent or undetected in the accepted die.

In practice, marginal dies would be identified in the following manner. Using the ATE as the numeric processor for the cluster method, the results of the wafer acceptance test would be used to calculated cluster values for each die. The accepted dies are then sorted in descending order by their cluster values. This is shown in Figure 49.



Die Failure Pattern

Rank	Cluster Value	Die #
1	2.61	78
2	2.58	79
3	2.51	41
4	2.51	62
...	...	...
101	0.90	15
102	0.80	2
103	0.76	186
104	0.61	13

Dies ranked by cluster value

Figure 49. A set of 104 accepted dies from a wafer test ranked in descending order by cluster value.

Assume that the MAL was calculated to be 0.90 by a previous set of tests. Those dies with cluster values greater than the MAL will be processed as usual. The dies with cluster values lower than the MAL, will be rejected or used in less demanding environments. In this case, the lowest four ranking dies in Figure 49 would be removed. Since most ATE are designed to mark dies that do not pass compliance tests, the dies designated as marginal by their cluster values, could be marked as well at this point. This then maintains continuity in normal operations.

Determining the Minimum Acceptance Level

The identification of marginal dies is performed indirectly and due to the number of failure modes possible on a wafer, is subject to inaccuracy. It is entirely possible that accepted dies with low cluster values could pass all quality assurance tests. As a result, it is important to set the MAL to the appropriate level such that the possible rejection of such dies is offset financially by the rejection of dies that are marginal.

To determine an appropriate MAL for a particular product (encapsulated die) on a stable fabrication line, the original die locations on the source wafers are tracked for each product. At each quality assurance screen, the failing products are recorded on a diagram of the wafer from which they were produced. At the end the quality assurance tests, the wafer diagram would be similiar to the one shown in Figure 50.

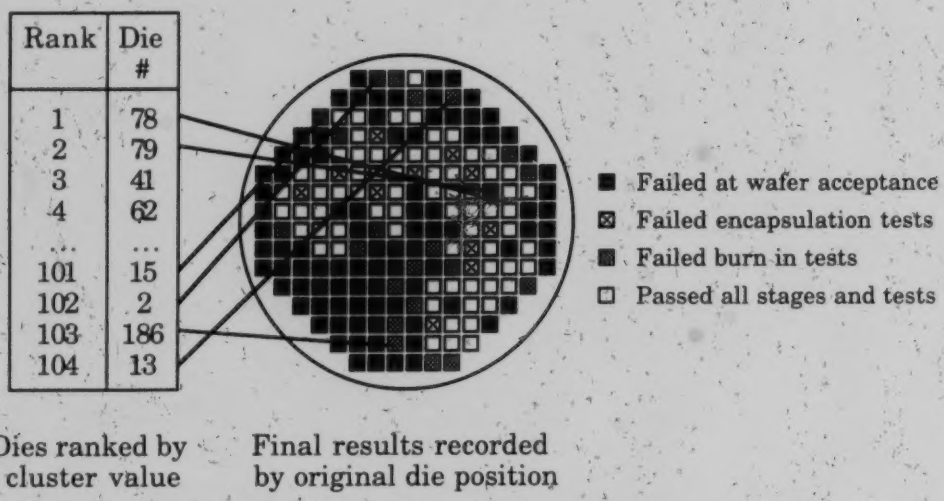


Figure 50. Final results recorded by orginal die position. The test results of each of the products is recorded in the original die position. The relationship between the final state of each product and the original die cluster value may now be established.

When the testing is complete, the optimum value of MAL must be determined. The optimum value of MAL would reject a significant portion of marginal dies (to save further processing costs) without rejecting a significant amount of high quality dies (the source of revenue). Table 12 shows that setting the MAL to 0.98 for the sample data set would cut off five marginal (grey) dies without rejecting a single high quality die (white). Setting the MAL to 1.22 would reject 11 marginal dies and one high quality die.

Table 12. The table shows the ranking of the accepted dies from Figure 50 in descending order of cluster values. The die categorization is: ⊠ – failed at encapsulation stage (as a direct result of the encapsulation process), ■ – failed during burn in tests, or □ – passed all stages and tests.

2.61 □	2.25 □	1.94 □	1.69 □□	1.26 ■
2.58 ■	2.24 □	1.93 □	1.59 □	1.25 ■
2.51 □⊠□	2.22 □□⊠⊠□	1.92 □	1.58 □	1.23 □
2.50 □□	2.20 □	1.91 □	1.57 □	1.22 ■
2.47 □	2.19 ■	1.90 □	1.53 ■	1.20 ■
2.43 ⊠□	2.15 □	1.88 □	1.47 ■□□	1.19 ■
2.39 □	2.14 □	1.87 □	1.45 □	1.18 ■
2.38 □□	2.12 □□□	1.86 □ ■	1.43 □□■	1.08 ■
2.37 □	2.08 □⊠	1.84 □	1.41 □	1.04 ■
2.36 ⊠	2.07 □□	1.82 □	1.40 ■ □	1.01 □
2.34 ⊠	2.06 □	1.80 □□	1.39 □	0.98 ■
2.31 ⊠	2.04 □□	1.78 □	1.37 □	0.90 ■
2.30 □□□⊠	1.98 ⊠	1.77 □	1.33 ■■	0.80 ■
2.29 □	1.97 □⊠	1.75 □	1.31 □	0.76 ■
2.26 □□□	1.95 □	1.70 □	1.29 □	0.61 ■

Choosing the most appropriate value of MAL becomes a trade off between conflicting objectives. If the value is low, the MAL will provide little benefit since few of the marginal dies will be rejected. For the data set shown in Table 12, only one marginal die has a value lower than 0.75. Therefore, the MAL must be set to at least 0.75 to have any noticeable effect. If the MAL is high, it will reject many of the high quality dies as well as the marginal dies.

Figure 51 shows several examples where the same set of dies are divided into two groups, those with cluster values greater than the MAL and those whose values are less. Each group shows the result of a change in MAL.

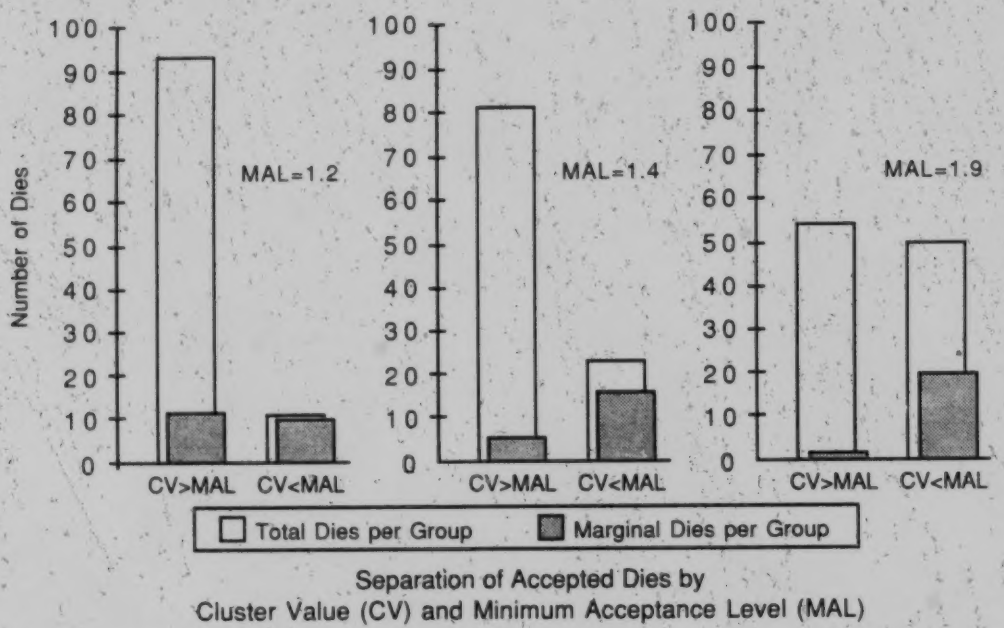


Figure 51. The accepted dies are divided based on their cluster values: those dies with cluster values > MAL, and dies with cluster values < MAL. Those in the first group will be processed, those in the second group will be discarded or processed for less demanding environments.

To find the optimum value for marginal die rejection, the full range of MAL values should be tested and the cost/benefit analyzed for each point. In Figure 52, the profit is graphed for a set of dies against a range of MAL values. As the value of MAL increases, the number of marginal dies in the final lot is reduced. This reduces the expenses involved in encapsulating and testing these dies. However, a portion of the high quality dies is removed as well which reduces the eventual number of

sales. The optimum value of MAL occurs where the financial gains of not processing the marginal dies are offset by the loss in revenue due to the removal of high quality dies.

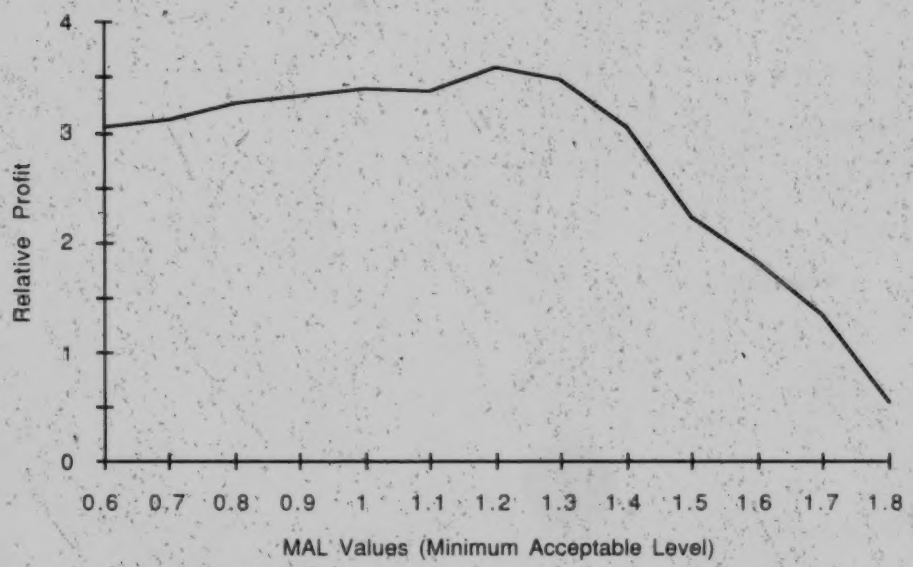


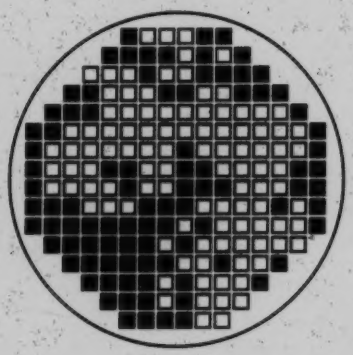
Figure 52. Financial return with increasing MAL. As the MAL value reaches the high end, a significant portion of the dies is removed. As a result, the revenue drops off sharply.

As shown in Figure 52, there is a gradual rise in profit until a level is reached where most of the marginal dies are removed. Thus, further increases in MAL will remove more of the high quality dies which reduces the number of revenue generating dies. For this data set, the ideal MAL is 1.22 which from Table 12 would eliminate 11 marginal dies and 1 high quality die. In practice, the MAL must be estimated over a set of wafers since the exact MAL values will vary from wafer to wafer.

Summarizing the philosophy behind the cost savings, if the cluster values are related to the success or failure of the dies at later processing stages,

then the early rejection of low cluster value dies reduces the expense of processing dies that may not survive.

A facility could extend the idea of the MAL to multiple values, and develop multiple cutoff points that represent quality confidence intervals. This is illustrated in Figure 53.



78 79	2.61 2.58	Level A
41 62	2.51 2.51	Level B
... 15	... 0.90	Level C
2 186 13	0.80 0.76 0.61	Level D
Failed Dies		Failed

Wafer Acceptance

Dies ranked by cluster value

Intervals developed through empircal studies

Figure 53. Using multiple MALs for discriminating between levels of cluster values. Each level could indicate a suitability for different quality requirements.

Tracking of the Fabrication Progress

The fabrication process may be tracked though charts of the wafer yield vs. the wafer cluster value. For each level of yield on the chart, there will be a minimum and a maximum cluster value (i.e., the number of ways **n** accepted dies may be arranged on a grid with **N** spaces). As a result, the chart has a hysteresis shape shown in Figure 54.

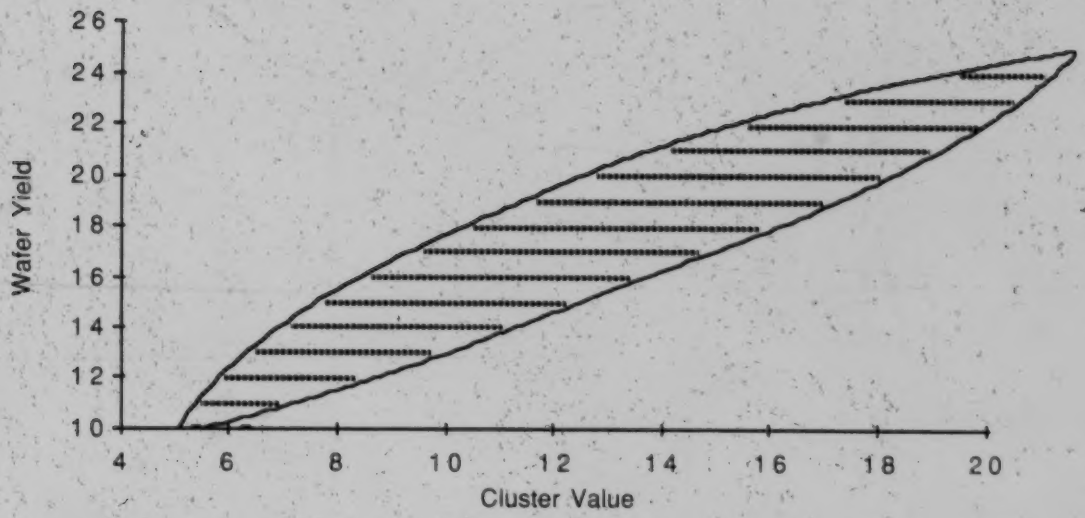


Figure 54. A product hysteresis curve. Every product (with a unique wafer grid) will have a unique hysteresis curve.

With two characteristics for the wafer, the yield and the cluster value, it is now easier to discern the nature of the changes that affect production.

CHAPTER 6

CONCLUSIONS

This thesis examined several models which are presently used for analyzing the performance of the IC fabrication process. Each of the existing models were analyzed for their shortcomings and the analysis formed the basis for the Cluster Model.

Chapter 1 presented an overview of the current research in models which analyze IC fabrication and IC failure. Chapter 2 then discussed the basis of current models with respect to defect size and distribution (i.e., defects are considered to be points which are distributed in a random but homogeneous manner). Wafer resistivity was then given as an example of defect distribution which countered these premises. From this, the cluster model was designed to deal with defects which may be distributed in a nonhomogeneous manner or whose dimensions may be as large as the wafer.

Chapter 3 described the formation and the use of the cluster model. The cluster model assigns quality confidence intervals to dies instead of the currently used rank of pass/fail. These intervals are assigned by examining each die in relation to the yield results of its neighbouring dies.

Chapter 4 showed the mathematical development of the Poisson distribution. It is suggested that the Poisson distribution is not universally applicable especially when defects are not distributed in a random homogeneous manner. The level of calculation error from the Poisson function was shown with respect to various quantities and arrangements of defects. The Poisson distribution model differs as well from the cluster model in that it examines defects whereas the cluster model analyzes yield. Chapter 5 showed applications of the cluster model in terms of cost savings measures and as a tracking tool. Finally, future directions for the model were discussed.

The cluster model was developed by analyzing in detail the foundations of existing models and contrasting those with physical processes found in the course of IC fabrication. Future inquiries of this nature will lead to an improved understanding of the fabrication system as a whole and ultimately to a greater understanding of the development of performance assessment models.

REFERENCES

[1] E.A. Amerasekera, and D.S. Campbell, **Failure Mechanisms in Semiconductor Devices**, John Wiley & Sons Ltd., 1987.

[2] P. Ghate, "Multilevel interconnection technology," Texas Instruments, 1984.

[3] S. M. Sze, **VLSI Technology**, 2nd ed., McGraw-Hill, 1988.

[4] N. Weste, and K. Eshraghian, **Principles of CMOS VLSI Design: A Systems Perspective**, Addison-Wesley, 1985.

[5] M. Walsh, **Choosing and Using CMOS**, McGraw Hill, 1985.

[6] M. Woods, "MOS VLSI reliability and yield trends," Proceedings of the IEEE, Vol. 74, No. 12, December 1986.

[7] A. Avizienis, and J. Laprie, "Dependable Computing: From Concepts to Design Diversity," Proceedings of the IEEE, Vol. 74, No. 5, May 1986.

[8] C.H. Stapper, "Correlation Analysis of Particle Clusters on Integrated Circuit Wafers," IBM J. Res. Develp. Vol. 31, No. 6, November 1987.

[9] C.H. Stapper, "Modeling of Integrated Circuit Defect Sensitivities," IBM J. Res. Develp. Vol. 27, No. 6, November 1983.

[10] A.V. Ferris-Prabhu, "Defect Size Variations and their Effect on the Critical Area of VLSI Devices," IEEE Journal of Solid State Circuits, Vol. sc-20, No. 4, August 1985.

[11] C.H. Stapper, "The effects of wafer to wafer defect density variations on integrated circuit defect and fault distributions," IBM J. Res. Develop. Vol. 29, No. 1, January 1985.

[12] Bertram, W.J., "Yield and Reliability," VLSI Technology, 2nd ed, S.M. Sze Ed. McGraw-Hill, 1988.

[13] F. Tsui, **LSI/VLSI Testability Design**, McGraw-Hill New York, 1986.

[14] C. Barney, "Wafer contour map helps correlate yield, process variables," Electronics Vol. 57, March 22, 1984.

[15] H. Suga, and K. Murai, "Effect of Bulk Defects in Silicon on SiO2 Film Breakdown," Emerging Semiconductor Technology ASTM. STD 960, D.C. Gupta and P.H. Langer, Eds., American Society for Testing Materials, 1986.

[16] Mazur, R.G., "Mapping Silicon Wafers by Spreading Resistance," Emerging Semiconductor Technology ASTM. STD 960, D.C. Gupta and P.H. Langer, Eds., American Society for Testing Materials, 1986.

[17] A.V. Ferris-Prabhu, "Radial Yield Variations in Semiconductor Wafers," IEEE Circuits and Devices Magazine, March 1987.

[18] N.D. Casper, and B.W. Soren, "Semiconductor Yield Enhancement through Particulate Control," Emerging Semiconductor Technology ASTM. STD 960, D.C. Gupta and P.H. Langer, Eds., American Society for Testing Materials, 1986.

[19] J. Bernard, "The IC Yield Problem: A Tentative Analysis for MOS/SOS Circuits," IEEE Transactions on Electron Devices, Vol ED-25, No. 8, August 1978.

[20] C.H. Stapper, "The Effects of Wafer to Wafer Defect Density Variations on Integrated Circuit Defect and Fault Distributions," IBM J. Res. Develp. Vol. 31, No. 6, November 1987.

[21] D.M.H. Walker, **Yield Simulation for Integrated Circuits**, Kluwer Academic Publishers, 1987.

[22] R. Petriz, "Current Status of Large Scale Integration Technology," IEEE Journal of Solid-State Circuits, SC-2(2), December, 1967.

[23] C.L. Mallory, et all, "Spatial Yield analysis in Integrated Circuit Manufacturing," Solid State Technology, November 1983

APPENDIX

TABLES USED IN THE DEVELOPMENT OF THE CLUSTER MODEL

Table A1. The following is a complete list of the 512 patterns listed in 86 rows. The first value in each row is the pattern that was used as part of the 86 unique wafers. The additional numbers in each row indicate patterns that are equivalent to the first and may be obtained through graphical pattern manipulation of the first pattern.

#	Wafer pattern															
1	0															
2	1	2	4	8	16	32	64	128	256							
3	3	6	9	18	24	36	48	72	144	192	288	384				
4	5	40	65	130	260	320										
5	7	56	73	146	292	448										
6	10	17	20	34	80	136	160	272								
7	11	19	22	25	26	38	50	52	88	152	176	200	208	304	400	416
8	12	33	66	96	129	132	258	264								
9	13	37	41	44	67	104	131	134	193	194	262	296	328	352	386	388
10	14	28	35	49	74	82	112	137	145	148	164	224	274	280	290	392
11	15	39	57	60	75	120	147	150	201	210	294	312	402	420	456	480
12	21	42	81	138	162	168	276	336								
13	23	58	89	154	178	184	308	464								
14	27	54	216	432												
15	29	43	46	53	83	139	166	202	209	232	278	344	368	404	418	424
16	30	51	90	153	180	240	306	408								
17	31	55	59	62	91	155	182	217	218	248	310	434	436	440	472	496
18	45	195	360	390												
19	47	61	203	211	376	406	422	488								
20	63	219	438	504												
21	88	257														
22	89	261	321	324												
23	70	76	100	196	259	265	289	385								
24	71	77	263	293	329	356	449	452								
25	78	228	291	393												
26	79	295	457	484												
27	84	273														
28	85	277	337	340												
29	86	92	116	212	275	281	305	401								
30	87	93	279	309	345	372	465	468								
31	94	244	307	409												
32	95	311	473	500												
33	97	133	268	322												
34	98	140	161	266												

35	**99**	141	165	225	270	330	354	396	
36	**101**	197	269	323	326	332	353	389	
37	**102**	204	267	417					
38	**103**	205	271	331	358	421	460	481	
39	**105**	135	300	450					
40	**106**	142	163	169	172	226	298	394	
41	**107**	143	167	233	302	428	458	482	
42	**108**	198	297	387					
43	**109**	199	301	361	364	391	451	454	
44	**110**	206	230	236	299	395	419	425	
45	**111**	207	303	423	459	486	489	492	
46	**113**	149	284	338					
47	**114**	156	177	282					
48	**115**	157	181	241	286	346	370	412	
49	**117**	213	285	339	342	348	369	405	
50	**118**	220	283	433					
51	**119**	221	287	347	374	437	476	497	
52	**121**	151	316	466					
53	**122**	158	179	185	188	242	314	410	
54	**123**	159	183	249	318	444	474	498	
55	**124**	214	313	403					
56	**125**	215	317	377	380	407	467	470	
57	**126**	222	246	252	315	411	435	441	
58	**127**	223	319	439	475	502	505	508	
59	**170**								
60	**171**	174	234	426					
61	**173**	227	362	398					
62	**175**	235	430	490					
63	**186**								
64	**187**	190	250	442					
65	**189**	243	378	414					
66	**191**	251	446	506					
67	**229**	334	355	397					
68	**231**	237	363	366	399	429	462	483	
69	**238**	427							
70	**239**	431	491	494					
71	**245**	350	371	413					
72	**247**	253	379	382	415	445	478	499	
73	**254**	443							
74	**255**	447	507	510					
75	**325**								
76	**327**	333	357	453					
77	**335**	359	461	485					
78	**341**								
79	**343**	349	373	469					
80	**351**	375	477	501					
81	**365**	455							
82	**367**	463	487	493					
83	**381**	471							
84	**383**	479	503	509					
85	**495**								
86	**511**								

Table A2. The following is a complete list of the die failure patterns for the 86 unique wafers.

0	0 0 0 0 0 0 0 0 0	70	0 0 1 0 0 0 1 1 0	111	0 0 1 1 0 1 1 1 1	229	0 1 1 1 0 0 1 0 1
1	0 0 0 0 0 0 0 0 1	71	0 0 1 0 0 0 1 1 1	113	0 0 1 1 1 0 0 0 1	231	0 1 1 1 0 0 1 1 1
3	0 0 0 0 0 0 0 1 1	78	0 0 1 0 0 1 1 1 0	114	0 0 1 1 1 0 0 1 0	238	0 1 1 1 0 1 1 1 0
5	0 0 0 0 0 0 1 0 1	79	0 0 1 0 0 1 1 1 1	115	0 0 1 1 1 0 0 1 1	239	0 1 1 1 0 1 1 1 1
7	0 0 0 0 0 0 1 1 1	84	0 0 1 0 1 0 1 0 0	117	0 0 1 1 1 0 1 0 1	245	0 1 1 1 1 0 1 0 1
10	0 0 0 0 0 1 0 1 0	85	0 0 1 0 1 0 1 0 1	118	0 0 1 1 1 0 1 1 0	247	0 1 1 1 1 0 1 1 1
11	0 0 0 0 0 1 0 1 1	86	0 0 1 0 1 0 1 1 0	119	0 0 1 1 1 0 1 1 1	254	0 1 1 1 1 1 1 1 0
12	0 0 0 0 0 1 1 0 0	87	0 0 1 0 1 0 1 1 1	121	0 0 1 1 1 1 0 0 1	255	0 1 1 1 1 1 1 1 1
13	0 0 0 0 0 1 1 0 1	94	0 0 1 0 1 1 1 1 0	122	0 0 1 1 1 1 0 1 0	325	1 0 1 0 0 0 1 0 1
14	0 0 0 0 0 1 1 1 0	95	0 0 1 0 1 1 1 1 1	123	0 0 1 1 1 1 0 1 1	327	1 0 1 0 0 0 1 1 1
15	0 0 0 0 0 1 1 1 1	97	0 0 1 1 0 0 0 0 1	124	0 0 1 1 1 1 1 0 0	335	1 0 1 0 0 1 1 1 1
21	0 0 0 0 1 0 1 0 1	98	0 0 1 1 0 0 0 1 0	125	0 0 1 1 1 1 1 0 1	341	1 0 1 0 1 0 1 0 1
23	0 0 0 0 1 0 1 1 1	99	0 0 1 1 0 0 0 1 1	126	0 0 1 1 1 1 1 1 0	343	1 0 1 0 1 0 1 1 1
27	0 0 0 0 1 1 0 1 1	101	0 0 1 1 0 0 1 0 1	127	0 0 1 1 1 1 1 1 1	351	1 0 1 0 1 1 1 1 1

29
0 0 0
0 1 1
1 0 1

30
0 0 0
0 1 1
1 1 0

31
0 0 0
0 1 1
1 1 1

45
0 0 0
1 0 1
1 0 1

47
0 0 0
1 0 1
1 1 1

63
0 0 0
1 1 1
1 1 1

68
0 0 1
0 0 0
1 0 0

69
0 0 1
0 0 0
1 0 1

102
0 0 1
1 0 0
1 1 0

103
0 0 1
1 0 0
1 1 1

105
0 0 1
1 0 1
0 0 1

106
0 0 1
1 0 1
0 1 0

107
0 0 1
1 0 1
0 1 1

108
0 0 1
1 0 1
1 0 0

109
0 0 1
1 0 1
1 0 1

110
0 0 1
1 0 1
1 1 0

170
0 1 0
1 0 1
0 1 0

171
0 1 0
1 0 1
0 1 1

173
0 1 0
1 0 1
1 0 1

175
0 1 0
1 0 1
1 1 1

186
0 1 0
1 1 1
0 1 0

187
0 1 0
1 1 1
0 1 1

189
0 1 0
1 1 1
1 0 1

191
0 1 0
1 1 1
1 1 1

365
1 0 1
1 0 1
1 0 1

367
1 0 1
1 0 1
1 1 1

381
1 0 1
1 1 1
1 0 1

383
1 0 1
1 1 1
1 1 1

495
1 1 1
1 0 1
1 1 1

511
1 1 1
1 1 1
1 1 1

Table A3. The following is a complete list of the proximity factors and cluster values for the 86 unique wafer patterns. The sort orders for each of the cluster value assignments is also listed. The cluster value formula that results from the inverse distance function is:

$$c_i = 3*F_0 + 1*F_1 + 0.70710678*F_2 + 0.5*F_3 + 0.4472136*F_4 + 0.35355339*F_5 \quad \text{(A1)}$$

The Gaussian function produces the following cluster value formula:

$$c_i = 1*F_0 + 0.77426368*F_1 + 0.59948425*F_2 + 0.35938137*F_3 + 0.27825594*F_4 + 0.12915497*F_5 \quad \text{(A2)}$$

							Cluster Values		Sort Order	
Wafer	F0	F1	F2	F3	F4	F5	Inv.	Gau.	Inv.	Gau.
0	0	0	0	0	0	0	0	0	1	1
1	1	0	0	0	0	0	3	1	2	2
3	2	2	0	0	0	0	8	3.549	7	7
5	2	0	0	2	0	0	7	2.719	5	5
7	3	4	0	2	0	0	14	6.816	16	16
10	2	0	2	0	0	0	7.414	3.199	6	6
11	3	4	2	0	0	0	14.414	7.296	17	17
12	2	0	0	0	2	0	6.894	2.557	4	4
13	3	2	0	2	2	0	12.894	5.824	14	13
14	3	2	2	0	2	0	13.309	6.304	15	15
15	4	6	2	2	2	0	21.309	11.120	34	34
21	3	0	4	2	0	0	12.828	6.117	13	14
23	4	6	4	2	0	0	21.828	11.762	36	36
27	4	8	4	0	0	0	22.828	12.592	37	37
29	4	4	4	2	2	0	20.723	10.770	33	33
30	4	6	4	0	2	0	21.723	11.600	35	35
31	5	10	6	2	2	0	31.137	17.615	58	58
45	4	4	0	4	4	0	19.789	9.648	27	24
47	5	8	4	4	4	0	29.617	16.143	52	52
63	6	14	8	4	4	0	41.446	24.186	74	74
68	2	0	0	0	0	2	6.707	2.258	3	3
69	3	0	0	4	0	2	11.707	4.696	8	8
70	3	2	0	0	2	2	12.602	5.363	12	11
71	4	4	0	4	2	2	19.602	9.349	23	23

Wafer	F0	F1	F2	F3	F4	F5	Cluster Values Inv.	Cluster Values Gau.	Sort Order Inv.	Sort Order Gau.
78	4	4	2	0	4	2	19.910	9.667	29	26
79	5	8	2	4	4	2	28.910	15.202	49	47
84	3	0	4	0	0	2	12.536	5.656	11	12
85	4	0	6	4	0	2	18.950	9.293	20	22
86	4	4	4	0	2	2	20.430	10.310	31	31
87	5	6	6	4	2	2	28.844	15.495	48	49
94	5	8	6	0	4	2	29.739	16.162	54	54
95	6	12	8	4	4	2	40.153	22.896	71	71
97	3	0	0	2	4	0	11.789	4.832	9	9
98	3	0	2	0	4	0	12.203	5.312	10	10
99	4	2	2	2	6	0	19.097	9.136	21	20
101	4	2	0	4	4	2	18.496	8.357	19	19
102	4	4	2	0	4	2	19.910	9.667	30	27
103	5	6	2	4	6	2	27.805	14.210	44	43
105	4	4	0	4	4	0	19.789	9.648	28	25
106	4	2	4	2	4	0	19.617	9.778	24	28
107	5	6	4	4	6	0	28.512	15.151	47	46
108	4	4	0	2	4	2	19.496	9.187	22	21
109	5	6	0	6	6	2	27.390	13.730	41	41
110	5	6	4	2	6	2	28.219	14.690	45	45
111	6	10	4	6	8	2	38.113	20.781	65	63
113	4	2	4	2	4	0	19.617	9.778	25	29
114	4	4	4	0	4	0	20.617	10.608	32	32
115	5	6	6	2	6	0	28.926	15.631	50	50
117	5	4	6	4	4	2	27.739	14.503	43	44
118	5	8	6	0	4	2	29.739	16.162	55	55
119	6	10	8	4	6	2	39.047	21.904	68	68
121	5	8	4	4	4	0	29.617	16.143	53	53
122	5	8	6	2	4	0	30.031	16.623	56	56
123	6	12	8	4	6	0	40.340	23.194	72	72
124	5	8	4	2	4	2	29.324	15.682	51	51
125	6	10	6	6	6	2	38.633	21.424	67	67
126	6	12	8	2	6	2	40.047	22.734	70	70
127	7	16	10	6	8	2	51.356	30.024	80	80
170	4	0	8	4	0	0	19.657	10.233	26	30
171	5	4	8	4	4	0	28.446	15.443	46	48
173	5	4	4	4	8	0	27.406	14.159	42	42
175	6	8	8	6	8	0	38.235	21.372	66	66
186	5	8	8	4	0	0	30.657	17.428	57	57
187	6	12	10	4	4	0	40.860	23.837	73	73
189	6	10	8	4	8	0	39.235	22.202	69	69
191	7	16	12	6	8	0	52.063	30.964	82	82
229	5	4	2	4	8	2	26.699	13.218	40	40
231	6	8	4	6	10	2	37.008	19.789	62	61
238	6	8	8	4	8	2	37.942	20.912	63	64
239	7	12	8	8	12	2	48.731	27.559	77	77

Wafer	F0	F1	F2	F3	F4	F5	Cluster Values		Sort Order	
							Inv.	Gau.	Inv.	Gau.
245	6	8	8	4	8	2	37.942	20.912	64	65
247	7	14	10	6	10	2	50.250	29.032	79	79
254	7	16	12	4	8	2	51.770	30.504	81	81
255	8	20	14	8	12	2	63.973	38.350	85	85
325	4	0	0	8	0	4	17.414	7.392	18	18
327	5	4	0	8	4	4	26.203	12.602	39	38
335	6	8	2	8	8	4	36.406	19.011	60	60
341	5	0	8	8	0	4	26.071	13.188	38	39
343	6	6	8	8	4	4	36.860	19.946	61	62
351	7	12	10	8	8	4	49.063	27.904	78	78
365	6	8	0	10	8	4	35.992	18.531	59	59
367	7	12	4	10	12	4	47.609	26.139	75	75
381	7	12	8	10	8	4	48.649	27.424	76	76
383	8	18	12	10	12	4	62.266	36.580	84	84
495	8	16	8	12	16	4	60.226	34.465	83	83
511	9	24	16	12	16	4	76.883	46.455	86	86